# Development and Characterization of a 300mm Dual-Side Alignment Stepper

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## ABSTRACT

A number of new packaging technologies are driving the demand for high performance dual-side alignment (DSA) on 300 mm lithography systems. Advanced system in package (SiP) techniques will require through silicon vias to allow very high density vertical interchip wiring of multiple device stacks. These through silicon vias need to be freely placed in the device which creates a requirement for tight registration of the back-to-front side alignment. In the MEMS area, wafer level packaging is being used for applications where the device must interact with the outside environment without performance restrictions from the packaging. An example is image sensor chips where the charge-coupled device is on the front side and the electrical interconnects to the signal processing die are on the back side. This application requires dual-side alignment on a 300 mm bonded silicon glass sandwich structure.

To support these packaging applications a new lithography stepper capable of dual-side alignment on 300 mm wafers has been developed. This stepper employs an innovative and flexible system for back-to-front side alignment to support a wide range of packaging applications. This paper discusses the design and integration of the alignment system on a broad band, low numerical aperture stepper. Experimental target capture for CMOS image sensor applications is shown. Dual-side overlay performance data on multiple wafers and lots is reviewed.

**Key Words:** Dual-side alignment, back-to-front alignment, system in package, wafer level packaging, MEMS, image sensors, 300mm wafers, lithography tool performance

## 1.0  INTRODUCTION

Dual-side wafer lithography has historically been used in the manufacturing of nanotechnology (MEMS) and high frequency devices. The MEMS applications include inertial accelerometers, pressure sensors, variable optical attenuators (VOAs), ink jet print heads, magnetic and optical-networking components and microshutter arrays [1, 2]. Dual-side patterning is employed in high frequency devices to minimize signal attenuation by thick metal deposition [1]. Most MEMS applications are fabricated using smaller diameter substrates due to low manufacturing volumes while high frequency devices are normally fabricated on III-V materials that are not available in larger wafer diameters [3]. As a result dual-side lithography equipment has been designed for handling 200 mm or smaller substrates.

Recently a number of new packaging technologies have started driving the demand for high performance dual-side alignment on 300 mm wafers. Advanced system in package (SiP) techniques require three dimensional integration of multiple layers of stacked planar devices [4]. These stacked devices are interconnected using through silicon vias to provide very high density vertical interchip wiring. The through silicon vias need to be freely placed in the devices which creates a requirement for tight registration of the back-to-front side alignment [5].

Three dimensional packaging designs greatly enhance the performance of logic circuits and minimize the form factor of the resulting package. Since each layer in the stack can have a specific function, it also allows the integration of otherwise incompatible technologies into the package [6]. A commercial application for three dimensional packaging is the camera module for cell phones [7]. Here the image sensor consists of a CMOS device on the front side with electrical interconnects on the back side connected to a signal processing die. This design allows a high fill factor for each pixel element of the detector, which minimizes signal noise and provides rapid processing time due to the short vertical interconnect to the processing die. In order to meet the volume and increased performance of present day camera modules, this application requires dual-side alignment on a 300 mm substrate.

# 2.0  SYSTEM DESIGN

## 2.1  Lithography System

The premier lithography systems used in advanced packaging applications are the Ultratech AP200 and AP300 wafer steppers. The steppers use the 1X Wynne-Dyson lens design employing mercury ghi-line illumination from 350 to 450 nm and having a 0.16 NA [8,9]. Dual-side alignment capability on these steppers gives end-users a powerful new tool for extending their wafer processing options. The AP300 uses a machine vision system (MVS) for wafer alignment, providing the flexibility in selection of alignment targets that is so important for advanced packaging applications

The new DSA system had to be designed to supplement the strengths of the AP300 without interfering with any existing stepper capabilities. Design of DSA operation was intended to leverage existing stepper capabilities and concepts. Job setup is analogous to constructing a front side EGA alignment application, but with a different camera selection. Like the main MVS wafer alignment system, the DSA alignment system can align to targets anywhere on the wafer.

## 2.2  DSA Design Trade-offs

In some new applications that are driving the need for DSA, the alignment target is embedded in the substrate. The device is processed on the front side of a silicon wafer as usual. The back side of the wafer is then thinned to between 500 and 50 μm, and a carrier is attached to the front side (device side) of the wafer to bring the total substrate thickness back to the standard wafer thickness. The challenge for a DSA stepper is to view this embedded alignment target, and expose a pattern on the back side of the wafer that is aligned to the device pattern on the front side. This scenario is illustrated in Figure 1.

Three approaches to dual-side alignment were considered: direct view, infrared (IR) with bottom side illumination, and IR with top side illumination. These three approaches are illustrated in Figure 2. In the first approach, prisms and/or relay optics are embedded in the wafer chuck, and an external optical system is used to form an image of the front side of the wafer on an image-capturing camera located elsewhere on the stepper. Multiple sets of prisms and/or relay optics can be embedded in the chuck to collect alignment data from multiple locations on a wafer. Ultratech's NT160 stepper was developed using this approach, for MEMS applications using 150mm and smaller substrates. In the second and third approaches, an alignment microscope uses infrared illumination to view through the silicon substrate to an alignment target on the front side of the wafer. The illumination can be directed from the bottom (front side) of the wafer (bottom illumination) or through the objective lens onto the top (back side) of the wafer (top illumination).

Each of these three approaches has significant advantages and disadvantages, which are listed in Table 1. One significant advantage of the IR top side illumination approach is that, because there are no optical elements embedded in the chuck, the alignment system can view targets at any location on the wafer. A full Enhanced Global Alignment (EGA) approach can be used to achieve better registration performance across the wafer. The biggest disadvantage of this approach is that the image contrast depends on the difference in reflectivity between the material used to pattern the alignment target and the neighboring materials. Furthermore, there can be no materials in the process stack between the substrate and the target layer that are opaque to infrared light. Figure 3 shows example images of alignment targets acquired using optical breadboard set-ups to evaluate the three approaches.

For the case where the alignment target is embedded in the substrate (see Figure 1), a direct view microscope would view the front side of the wafer through the carrier and bonding agent. This puts significant constraints on the optical properties, uniformity, and consistency of the carrier and adhesive, as these components now become part of the optical path of the alignment system. For this reason, and because of the flexibility of the IR approach in selecting and locating alignment targets, the IR top side illumination approach was chosen for the implementation of DSA on the AP200/AP300 stepper

## 2.3  DSA Implementation

The IR DSA system was designed to achieve back-to-front overlay of less than 2 μm (mean + 3σ) over a full 300 mm wafer and minimize the impact on throughput relative to front side alignment. Substrates could be from 50 to 200 μm thick silicon, polished on the back side with metal targets up to 100 μm by 100 μm on the front side. Other key factors that impacted design choices were tight space constraints, cost, and schedule. The existing machine vision alignment system was leveraged to minimize new development of image processing, control hardware, and system level software.

The primary concept decisions concentrated on illumination wavelength, illumination source type, image sensor type, and optical design. A shorter illumination wavelength allows higher optical resolution, but the wavelength must be long enough to transmit efficiently through silicon. The illumination bandwidth must be chosen carefully to efficiently illuminate the wafer target. This is because the illumination light reflects strongly from the two silicon surfaces, contributing to the background level that reduces contrast in the image. The overlay error budget required an alignment system capture repeatability of less than 0.25 μm. To achieve this requires image data with high signal-to-noise ratio, high edge-sharpness, maximum number of pixels, and a high-accuracy alignment algorithm.

Several options for the type of light source were considered. A broad-spectrum incandescent lamp, filtered to the appropriate wavelength band, would provide the highest irradiance, which could be important for substrates with low contrast and high attenuation. However, this type of source is relatively expensive, is highly inefficient and has a limited bulb lifetime. Most of the emitted spectrum is not used, and this energy is lost as heat, which must be managed. Alternatively, light emitting diodes (LEDs) are compact, long-lived, and highly efficient, but in contrast, they have limited brightness and less uniform output. Successful implementation of LEDs for this application depended on providing the optimum wavelength and sufficient irradiance on the target to produce a high contrast, low noise image.

The choice of image sensor was linked to the choice of light source. Silicon-based image sensors are compact, low cost, and have very good performance, but their response is severely degraded above 900 nm wavelength where silicon begins to transmit. InGaAs based image sensors have much higher sensitivity above 900 nm, but are relatively large, have lower pixel density and are much higher in cost.

For this application, a combination of silicon image sensor and LED light source was identified that successfully met the design criteria. The selected camera fit in the available space and was directly compatible with the existing image processing board. Three standard inexpensive LEDs were combined using a fiber bundle to provide the required illumination irradiance and uniformity at the wafer. This feature also allows the illumination source to be placed remotely to minimize heating effects and enhance serviceability.

The imaging objective for the microscope was custom designed to meet the requirements for working distance, space constraint, illumination numerical aperture, magnification and image quality. A conceptual layout is shown in Figure 4. The microscope has coaxial bright field illumination inserted into the optical path by a beam splitter. The light passes through the objective to the substrate and is reflected by the wafer target. The light returns through the imaging objective and reflects off two folding mirrors to reach the image sensor. Because it is looking through the silicon substrate, the microscope requires a minimum of 2 mm of working distance from the last element to the image plane. The design was constrained to a total physical height of 31 mm and an optical path length of less than 200 mm requiring compact packaging. The numerical aperture of the microscope objective was matched to the NA of the illumination system for maximum light transfer efficiency. The magnification is chosen to optimize the trade-off between image field size and resolution. The objective is designed to have very low distortion and to yield diffraction limited image quality.

The DSA microscope field was located on the stepper as close as possible to the top side MVS to minimize the wafer stage move distance and maximize mechanical stability. The arrangement is shown in Figure 5. The top side MVS looks through the projection lens and uses a reticle feature as its alignment reference. A wafer stage artifact and the MVS alignment system are used to reference the wafer stage coordinate system to the reticle coordinate system. The artifact is also used to reference the center pixel of the DSA image sensor to the reticle coordinate system resulting in an accurately calibrated offset distance between the center of the reticle target and the center of the DSA sensor.

# 3.0 EXPERIMENTAL METHODS

## 3.1 Wafer Processing

An Ultratech AP300 wafer stepper, equipped with the new DSA system, was used to expose 200 mm and 300 mm diameter SEMI standard silicon wafers. The wafers were coated with one micron thick Fujifilm OiR906 photoresist, exposed on the AP300 using broadband mercury ghi-line illumination, and immersion developed in 2.38% TMAH.

## 3.2 Metrology

In 2003, Ultratech introduced the UltraMet 100, a metrology tool designed to measure registration between layers printed on two sides of a wafer [10, 11] for substrates up to 150mm in diameter. To support the new DSA system designed for the Unity AP stepper platform, a method was needed to measure back-to-front registration on 200 mm and 300 mm wafers. Furthermore, back-to-front registration metrology is more challenging in the current application, because the front side pattern is embedded in a substrate sandwich, rather than sitting on the surface of the processed wafer.

Two methods were used to evaluate and qualify overlay performance using the DSA system on the AP300 stepper: a single-pass test and a double-pass test, where single and double refer to the number of aligned layers. The single-pass test uses the off-axis DSA system in a top side alignment mode. In this test, a blank photoresist-coated wafer is first patterned with a blind-stepped reference layer. The DSA system then aligns the patterned wafer to a second layer with a specific offset in order to create overlaid metrology structures. While this test does not exercise the ability of the off-axis IR optics to view alignment targets through the Si substrate, it can be used as a baseline test to verify and monitor the calibration and stability of the off-axis alignment system, independent of front side target quality and process variation.

In the double-pass test, artifact wafers containing embedded (front side) alignment targets are used. Two layers are sequentially aligned and exposed: the first layer is aligned to the embedded front side target and exposed on the resist coated back side with the wafer oriented at 0° rotation, and the second layer is aligned and exposed with the wafer oriented at 180° rotation. The test reticle was designed so that the nesting of the 0° and 180° patterns create overlaid metrology structures. Since the structure is the result of two alignments and two exposures, a repeating offset error in alignment doubles the error in the metrology structure. Thus by measuring the misregistration between the two aligned resist layers, we can estimate the overlay error between the front and back side.

For example, considering a box-in-frame metrology structure, when the wafer is rotated, the second pattern is designed to place a box at the center of a frame that was printed in the first aligned layer, assuming perfect alignment in both cases. However, if there is a misregistration in one or both layers, the box will be decentered in the frame by the combined alignment error. For a systematic overlay error, the misregistration printed in the second pass will be equal and opposite of the misregistration of the first pass, thus doubling the error seen between the box and frame. For random errors, the total error can be estimated by adding the two errors in quadrature. This is illustrated in Figure 6.

Total overlay error is generally reported as the mean + 3σ of misregistration measured at multiple sites within a field, on multiple fields on a wafer, and for multiple wafers. In the double-pass test, the mean error represents the systematic error for this set of wafers, and the 3σ represents the distribution of random errors, so total overlay error can be estimated as:

$$(\text{mean} + 3\sigma)_{\text{SP}} = \frac{(\text{mean})_{\text{DP}}}{2} + \frac{(3\sigma)_{\text{DP}}}{\sqrt{2}} \qquad (1)$$

where SP is the single pass and DP is the double pass test.

The test reticle designed and used for this study contains metrology structures for both the single-pass and double-pass tests. Metrology structures consist of standard box-in-frame patterns as well as a pattern of overlaid crosses. The latter structures are used for a vision-based metrology routine that runs on the AP300 stepper, and this technique was used for the results reported in this paper.

Figure 7 shows examples of the overlaid patterns. Figure 7a shows a pattern that was created when an artifact wafer was patterned with a single aligned layer. In this image acquired using the DSA system, the central cross has been patterned in metal on the front side of the wafer, and is viewed from the back side through the wafer. The four outer crosses are patterned in photoresist on the back side of the wafer after wafer alignment. Figure 7b shows a pattern on the resist coated back side that was created using the double-pass overlay test. The central cross was patterned in the first aligned layer, and the four outer crosses were patterned after the wafer was rotated 180° and aligned using the DSA system.

## 3.3 Test Wafers

Artifact test wafers were created to evaluate and qualify overlay performance using DSA alignment. The artifact wafers were coated with aluminum on their front side and then pattered using the DSA test reticle. The pattern was etched into the metal layer using a wet-etch process, and then the wafers were thinned to 100 μm and attached to a carrier with the aluminum side (front) facing the carrier. The resultant substrate-metal-carrier sandwich was approximately 725 μm thick. Because of

limitations in wafer processing capabilities, the quality of the alignment targets on the test wafers is inferior to what we expect to see in production DSA wafers. Figures 8a and 8b show typical alignment targets from a test wafer and from a short-loop product wafer, respectively.

# 4.0  RESULTS AND DISCUSSIONS

## 4.1  Imaging and Capture Repeatability

The optical design criteria for the DSA system are described above in Section 2.3. The performance resulting from that design is shown in Figure 9. Figure 9a shows an image acquired from a representative short-loop wafer with embedded front side alignment targets. This image was acquired using the breadboard system assembled to evaluate feasibility. Figure 9b shows an image of a similar target on a similar wafer acquired using the prototype DSA system as implemented on the AP300 stepper.

Target capture repeatability is an important contributor to the overlay error budget for DSA. Uncertainty in the found position of an alignment target contributes directly to the calculated EGA grid when aligning a wafer. Target capture repeatability is affected by image signal-to-noise ratio and image edge sharpness. In order to achieve the overall overlay specification of 2 microns, the system was designed so that capture repeatability would not exceed 0.25 $\mu$m 3$\sigma$.

Capture repeatability tests were performed on artifact wafers created for overlay metrology and on a sample short-loop product wafer from a potential end-user. At eight different locations on a wafer, an alignment target is repeatedly captured from a stationary position. Variation in the found position is caused by the factors described above, and is a measure of the target capture repeatability. Data was collected for 30 seconds in each case, and this time period allowed approximately 170 samples. The 3$\sigma$ variation was calculated for each set of data from a single alignment target, and capture repeatability was reported as the highest from the eight measured sites. For a test wafer, the worst case 3$\sigma$ on one wafer was 194 nm. For a short loop product wafer, the worst case 3$\sigma$ on one wafer was 49 nm. In both cases, the capture repeatability of the DSA alignment system is sufficient to support the overlay specification of 2 $\mu$m.

## 4.2  Overlay with DSA

Results of DSA overlay testing are shown in Figure 10, Figure 11, and Figure 12.

Figure 10 shows the results for the single-pass overlay test performed on 200 mm wafers on an AP300 stepper at Ultratech. Eleven runs were measured over a period of 20 days. Results are reported as mean + 3$\sigma$ of the misregistration measured at 3 sites/field, 22 fields/wafer, and 4 wafers/run. The last two data points on this graph were measured on 300 mm wafers, 3 sites/field, 52 fields/wafer, 4 wafers/run. The line at 2.0 $\mu$m shows the overlay design criteria.

Figure 11 shows the results from the double-pass overlay test performed on 200 mm artifact wafers on the same AP300 at Ultratech. Eight runs were measured over a period of 20 days. Preceding runs were used to calibrate system offsets. No further stepper adjustments were made during the period of the runs shown in the graph.

Figure 12 shows the results from the double-pass overlay test performed on a different set of 200 mm artifact wafers on a different AP300 stepper at a field location. Five runs were measured over a period of 30 days. Preceding runs were used to calibrate system offsets. No further stepper adjustments were made during the period of the runs shown in the graph.

The results of the double-pass tests have been calculated from the raw data to estimate equivalent single-pass performance as described above. In all cases the measured overlay is between 1 and 1.5 $\mu$m, mean + 3$\sigma$.

# 5.0  CONCLUSIONS

A dual-side alignment system was designed for the Ultratech Unity Platform and integrated on an AP300 wafer stepper. A technique was developed to measure back-to-front overlay when no through-wafer metrology tool is available. This was used to demonstrate that the overlay performance of the dual-side alignment system fell well within the system specification of 2.0 $\mu$m, mean + 3$\sigma$.

# 6.0 ACKNOWLEDGEMENTS

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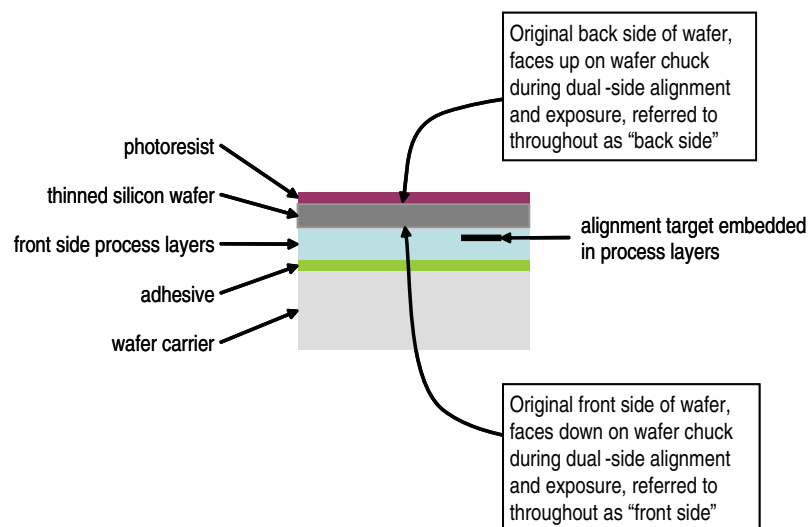


**Figure 1**: A DSA stepper is used to view an embedded alignment target, and expose a pattern on the back of the wafer that is aligned to the device pattern on the front side of the wafer.

| Approach | Advantages | Disadvantages |
|---|---|---|
| Direct View | Previous implementation exists on Ultratech's NT160 wafer stepper | ● Requires tight control of optical properties of carrier and adhesive<br><br>● Limits alignment target location<br><br>● Compromises flatness of wafer on chuck which impacts local overlay<br><br>● Higher system complexity for subsystem alignment and calibration<br><br>● Cannot tolerate additional metal layers between target layer and glass |
| IR-bottom side Illumination | Image formed by shadowing of metal target provides high image contrast | ● Requires some control of optical properties of carrier and adhesive<br><br>● Limits alignment target location<br><br>● Compromises flatness of wafer on chuck which impacts local overlay<br><br>● Higher system complexity for subsystem alignment and calibration<br><br>● Cannot tolerate additional metal layers either above or below target layer |
| IR-top side Illumination | ● Can view alignment targets anywhere on wafer<br><br>● No constraints on optical properties of carrier and adhesive<br><br>● No windows in wafer chuck results in no local loss in overlay performance | ● Image formed in camera by reflection off of metal target could result in lower image contrast<br><br>● Cannot tolerate additional metal layers between target layer and silicon |

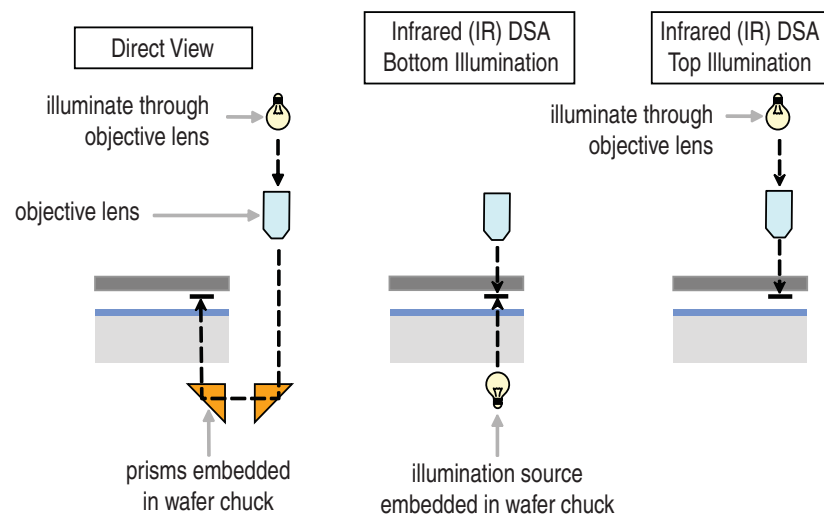**Table 1:** Advantages and Disadvantages of three methods of DSA.

**Figure 2**: Three approaches to dual-side alignment were considered: direct view, infrared (IR) with bottom side illumination, and IR with top side illumination.
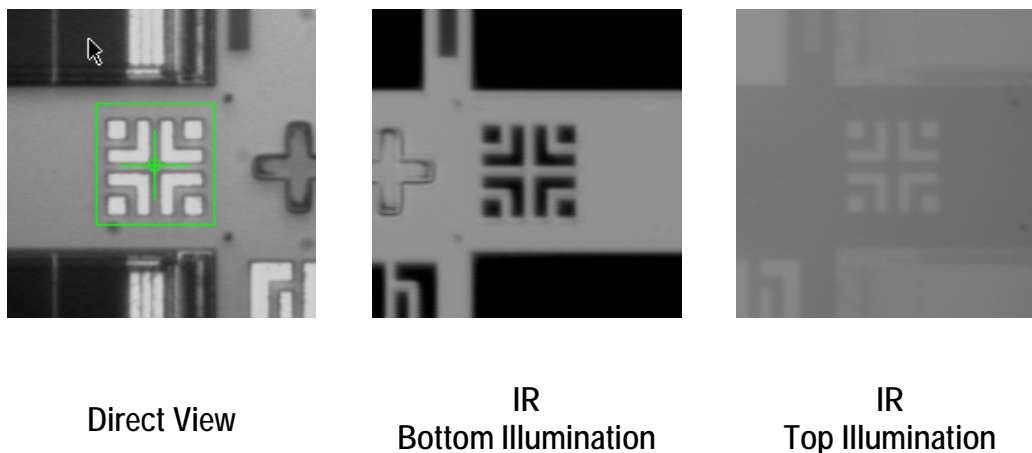
**Direct View**

**IR
Bottom Illumination**

**IR
Top Illumination**

**Figure 3**: Comparison of images of alignment targets acquired using the three DSA approaches.



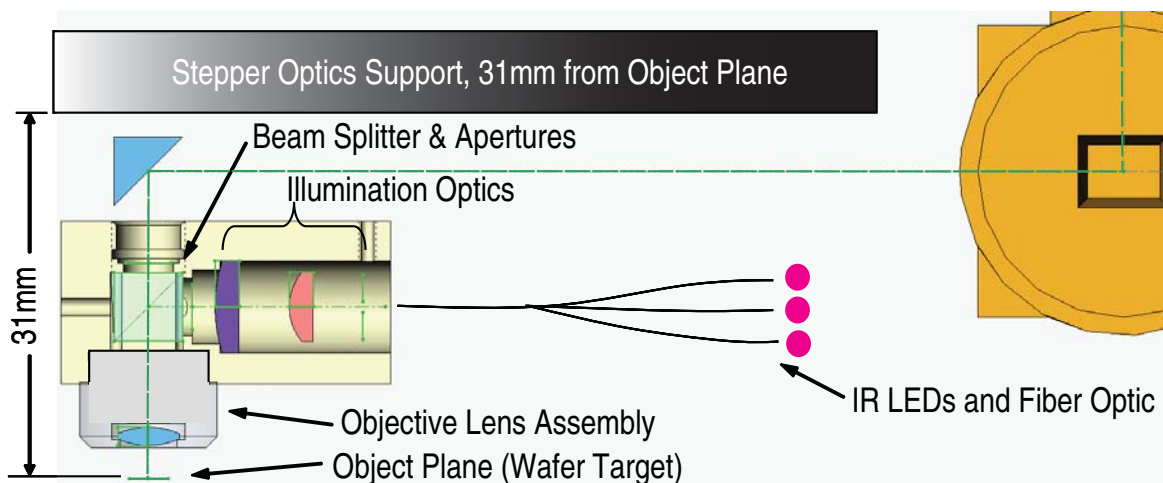Stepper Optics Support, 31mm from Object Plane

Beam Splitter & Apertures

Illumination Optics

31mm

IR LEDs and Fiber Optic

Objective Lens Assembly

Object Plane (Wafer Target)

**Figure 4**: The imaging objective for the DSA microscope was custom designed to meet the requirements for working distance, space constraint, illumination numerical aperture, magnification and image quality.



DSA field

MVS field

Offset
distance
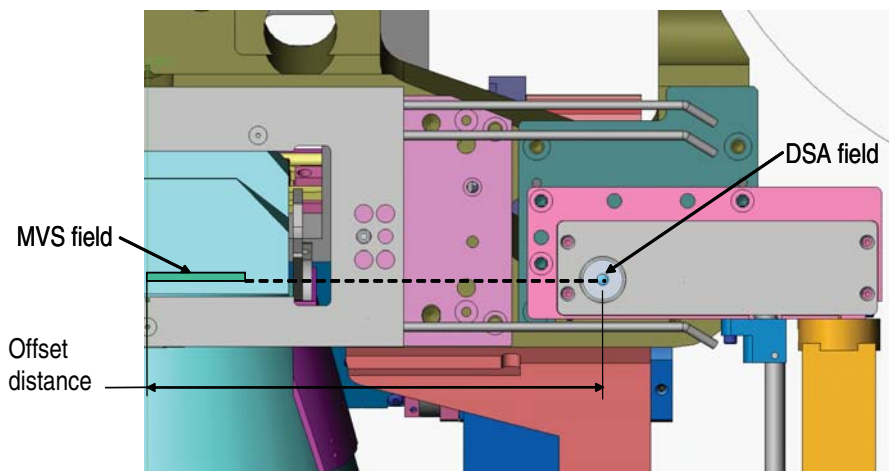
**Figure 5**: Bottom view of DSA microscope on stepper looking up from the wafer. The figure shows the top side MVS alignment field position relative to the back side DSA microscope field.

(a) Systemic Errors         (b) Random Errors
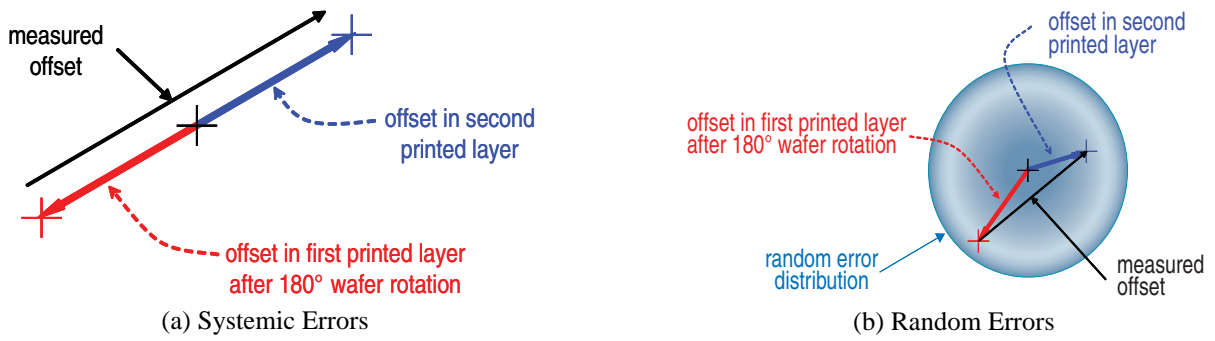
**Figure 6**: (a) For a systematic overlay error, the misregistration printed in the second pass will be equal and opposite to the misregistration of the first pass. (b) The random errors add in quadrature.
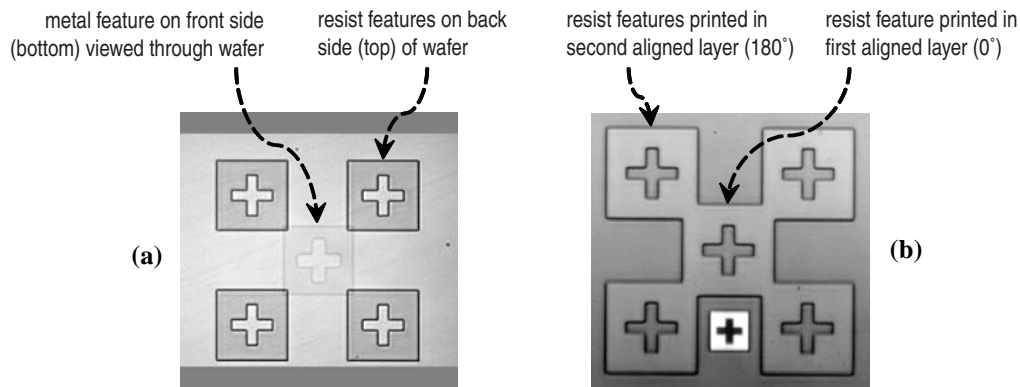


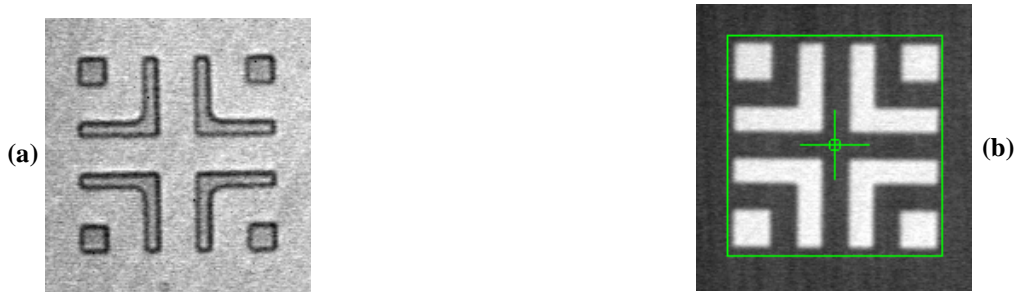**Figure 7**: Pattern overlaid metrology structures: (a) back-to-front and (b) after double-pass overlay test.



**Figure 8**: Example alignment targets viewed through wafer. (a) alignment target from test wafer (b) alignment target from short loop product wafer



**Figure 9**: Image quality comparison for (a) alignment target viewed on breadboard system and (b) alignment target viewed on DSA system on stepper.
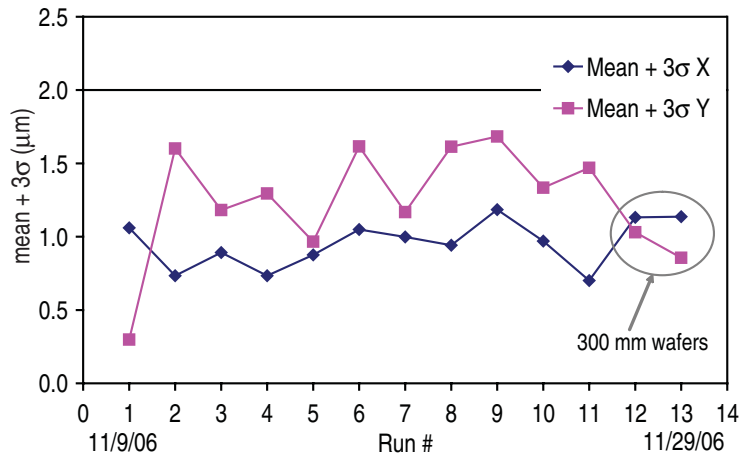
**Figure 10**: Results for the single-pass overlay test performed on 200 mm wafers on an AP300 stepper at Ultratech. The line at 2.0 μm shows the overlay design criteria.
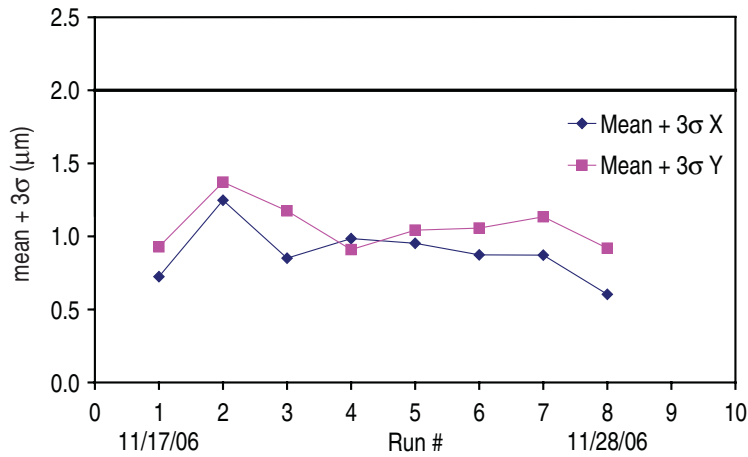


**Figure 11**: Results from the double-pass overlay test performed on 200 mm artifact wafers on the same AP300 at Ultratech.
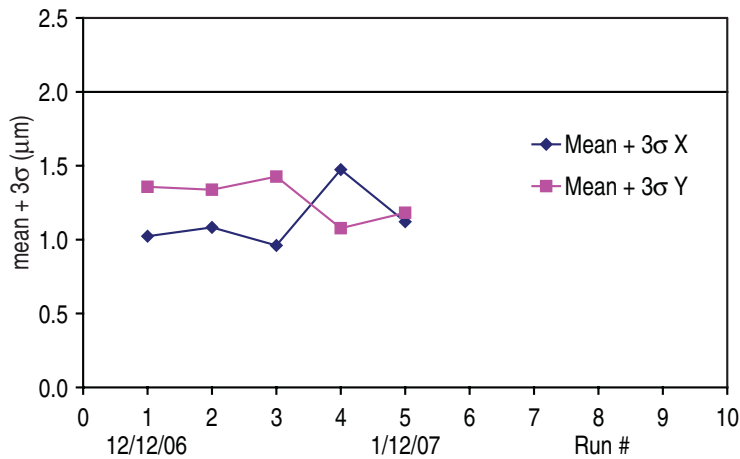


**Figure 12**: Results from the double-pass overlay test performed on a different set of 200 mm artifact wafers on a different AP300 stepper at a field location.