LITHOGRAPHY CHALLENGES AND CONSIDERATIONS FOR EMERGING FAN-OUT WAFER LEVEL PACKAGING APPLICATIONS

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ABSTRACT
Leading edge consumer electronic products demand innovative and cost effective packaging solutions. While front end silicon technologies have followed Moore's law by device scaling, the back end infrastructure has lagged in similar advancements. This has created an interconnect gap whereby the signal speed achieved on the silicon side is significantly higher than the speed achieved on the printed circuit boards. Innovative advancements such as fan-out wafer level packaging technology deliver robust packaging solutions to meet the performance and reliability requirements for leading edge devices.

Fan-out wafer level packaging technology was introduced to addresses the pad limitation consideration with traditional wafer level packaging while delivering miniaturization and potential low cost packaging advantages. It enables high performance bump interconnects with input/output (I/O) counts exceeding the capacity of the original front end chip size. The bump array area for each chip is increased by populating a composite wafer with tested good die at a larger repeat pitch than the original die. The reconstituted fan-out wafer has the size and shape of standard silicon wafers allowing the use of existing wafer processing equipment. For compatibility with planar processing steps the die surface needs to be coplanar with the wafer molding compound. Also the X, Y, and Theta positioning of each die needs to be accurate within the grid to maintain registration performance while patterning multiple die per exposure.

Die positioning control within the reconstituted wafer is one of the key factors affecting the downstream process requirements. While considerable improvements have been made with the die pick and place equipment, it is difficult to control the shift of the silicon die during the compression molding process. This creates significant challenges during the subsequent photolithography process steps. This paper discusses sources of registration error for patterning on reconstituted wafers, and demonstrates that registration improvements to well below 10 µm can be achieved using a stepper exposure tool. Experimental data from fan-out test wafers demonstrate various lithographic approaches to minimize registration errors.

Key words: Fan-out wafer level packaging, reconstituted wafers, lithographic registration errors.

INTRODUCTION
Despite the recent economic slowdown, semiconductor manufacturers are witnessing positive growth in the mobile phone market segment. Within the mobile market smart phone shipments have remained relatively strong. Smart phones have experienced a steady increase in adoption of various features such as cameras, global positioning systems (GPS), and mobile televisions [1]. To effectively address the performance and form factor considerations, leading-edge IC suppliers have migrated to tighter design rules for front end silicon manufacturing. However, there has not been a similar technology scaling effort in the packaging arena. The near term packaging requirements have been met using incremental improvements of current packaging methods. However, new packaging solutions are being developed to meet leading edge device scaling requirements. The widely used wire bond packaging method for connecting silicon chips to the mother board is poorly suited for leading edge devices due to low signal speed and dense wire routing considerations. Traditional Wafer Level Packaging (WLP) solutions are fan-in solutions which provide limited pad area for small die sizes. The introduction of fan-out WLP technology addresses the pad area limitation of traditional WLP while delivering miniaturization and potential low-cost packaging advantages. In addition, the fan-out WLP technology can effectively leverage the current flip chip and WLP equipment infrastructure thereby creating a cost-effective technology solution [2]. This technology supports placing multiple types of chips on the reconstituted wafer.

One of the key process steps for fan-out technology is the reconfiguration of probed good die into a carrier. The resulting panel is processed using thin-film technologies such as sputtering, photolithography and electroplating. The final interconnect process step is the ball drop process followed by singulation and testing of packages [3].

The panel fabrication method used in this study uses a molding compound for the carrier. The reconstituted fan-out wafer has the size and shape of standard silicon wafers allowing the use of existing wafer processing equipment. For compatibility with planar processing steps the die surface is coplanar with the wafer molding compound.

Die positioning control within the mold compound on the panel is one of the key factors affecting the downstream process requirements. Unlike a typical front end silicon wafer, the die within the reconstituted wafer can significantly shift in position from the designed systematic array. The chip locations have a residual error component due to the limited accuracy and precision of the pick and place tool. However the major source of error comes from shrinkage of the molding compound material during the compression molding process. This creates significant challenges in aligning subsequent metal layers to the device contacts. For backend patterning, full wafer alignment tools (aligner) and step-and-repeat tools (stepper) are common optical patterning tools having different overlay performance characteristics. The full wafer aligner places the mask and wafer in close proximity and exposes the wafer in one shot, whereas the stepper exposes a smaller repeating pattern across the wafer. The aligner relies on the stability of the mask plate pattern to get repeatable results but does not have adjustments for dealing with common wafer distortions. The step-and-repeat exposure sequence has flexibility for dealing with wafer distortions caused by processing and patterning mismatch [4, 5].

As a remedy, some device manufacturers using full wafer aligners to process fan-out wafers are introducing chip designs with large passivation openings to accommodate the overlay error. However, this limits shrinking geometries for future device generations and becomes cost prohibitive. As fan-out technology advances, the requirements for overlay registration and individual die placements will tighten, placing increased demands on lithographic techniques, and die placement accuracy and precision in the reconstituted wafer. The lack of adjustment for these errors makes aligners a poor choice to meet the demands of advancing fan-out technology.

ALIGNMENT STRATEGIES

By using stepper technology it is possible to take advantage of various alignment strategies to better address the die placement errors on the fan-out wafers. This allows support for fan-out WLP technology for leading-edge design rules with smaller pad openings and tighter overlay requirements.

Optimizing the alignment on a stepper requires breaking down error sources into systematic components. Overlay error can be split into intrafield (within a shot) and interfield (grid) effects [5]. Intrafield errors include zero-order effects such as X and Y mean, and linear effects such as field rotation, orthogonality, and scale (magnification) [5,6]. These comprise the bulk of intrafield matching errors. The maximum registration error from a linear intrafield error depends on the size of the exposure field. Thus the full wafer aligner has the greatest sensitivity to linear errors since this method uses a single exposure field for the whole wafer.

For a stepper, interfield effects relate to the optimum arrangement of multiple shots. Note that a full set of linear interfield corrections are automatically calculated from Enhanced Global Alignment (EGA) measurements, and it usually is not necessary to offset the calculated grid terms for non-critical bump applications [6].

For productivity, the stepper exposure field size should be maximized to reduce the number of shots required to expose the entire wafer. For typical fan-out die sizes this means putting multiple die within a field. Therefore the grid scaling needs to closely match the stepper field scaling to effectively utilize the largest field size. For fields containing multiple die the random placement error of the die with respect to each other is included in the total overlay budget. Compensation for random die placement error requires aligning to and exposure of a single die at a time. However, while this yields the smallest overlay error it may be impractical for small die because of the low system throughput and productivity.

The alignment process itself introduces additional overlay errors. The key parameters for alignment are the alignment locations and number of samples. For a full wafer aligner two points are measured to get X, Y, and rotation information. Since X is the average of two measurements the X mean estimate is less sensitive to placement error of a single die. However Y mean and Theta will incorporate the full effect of die placement error at the alignment site.

The stepper model includes additional modeling terms to define a linear grid and thus a fully constrained model can be determined from three measurement points, but more points are typically used to suppress the effect of individual die placement error. Nine site EGA is used in this investigation to obtain a better estimate of the underlying wafer grid.

EXPERIMENTAL METHODS

A total of ten 200 mm diameter fan-out test wafers were provided for this study. The fan-out wafers consist of 390 individual device die placed in molding compound and also contain two die that serve as left and right alignment marks for the full wafer aligner. Inter-die pitch is 8.16 mm x 8.16 mm. The wafers were initially fully characterized by an absolute measurement of the die positions using a Nikon VMR3030 microscope. The tool used two global alignment marks to define a coordinate system for the reconstituted wafer. With respect to that the positional measurement of two marks placed in opposite corners of each chip leads (within the tool precision of 1µm absolute) to the pick and place die shift in X, Y and rotation error for each individual die compared to the mask layout file. These data are used to characterize overlay performance on a full wafer aligner.

A subset of three wafers were used to investigate how grid matching and die placement errors affect the overlay using various field sizes and alignment modes The three wafers selected for the investigation represent the spread of die placement distributions found in the full set of ten. Only three wafers were used to minimize the extensive time required for all of the overlay metrology measurements

Lithography for this study was performed using an Ultratech Unity AP300 Wafer Stepper. This system has a 0.16 numerical aperture (NA) and employs Mercury ghi-line illumination from 350 to 450 nm. The low NA and broadband illumination spectrum of the stepper provides a large depth of focus and minimizes the standing wave pattern in the photoresist side wall near the substrate [7]. The exposure dose and focus offsets of the stepper were optimized for 4 µm features in the photoresist.

Two 1X reticles were made to accommodate four different field sizes for the stepper, covering 15 (5x3), 6 (3x2), 4 (2x2), and 1 (1x1) device die, respectively. Wafer layouts were then constructed to expose all 390 die with the fewest number of exposure shots, as shown in figure 1. The 1x1 die array (reference wafer) has 390 exposure shots; the 2x2 die array has 103 exposure shots, and the 5x3 die array has 34 exposure shots.

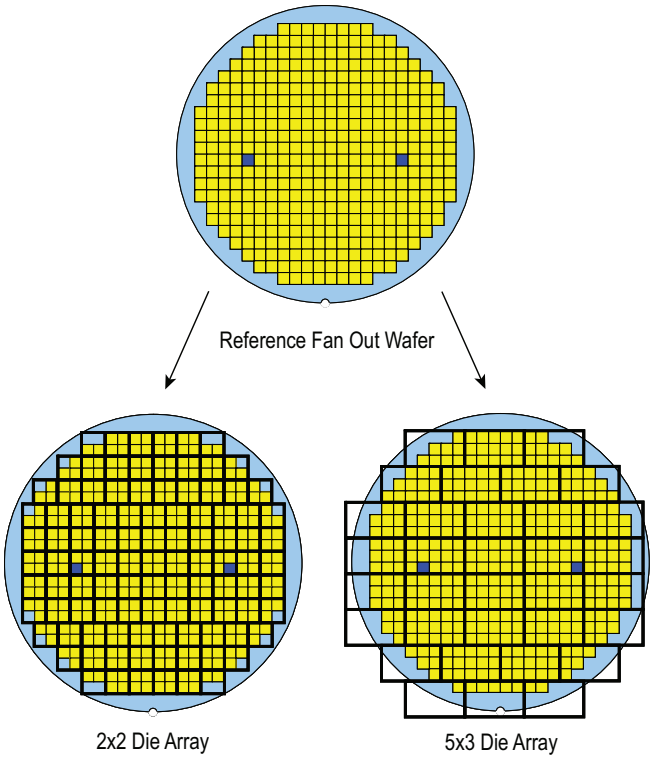

Figure 1. Arrangement of product die on the reference fan-out wafer and matching layouts using two field sizes.

The set of the three fan-out wafers were run multiple times on the stepper to evaluate overlay using different alignment strategies. Four experimental runs tested two field sizes (5x3 die array, 2x2 die array) and two alignment modes, EGA and Site-by-Site (SxS). Each field size uses a matching reticle field. The 5x3 die array is the largest to fit into the maximum exposure field of the stepper (44 by 26.7 mm). The 2x2 die array was chosen to provide more matching flexibility for the fan-out wafer. A field size with a 1x1 die array would have the lowest throughput. As we will discuss later, the overlay performance of a 1x1 die field scenario can be derived from the 2x2 die field measurements. Evaluation consists of measurements of resist to wafer pattern overlay using a pattern recognition technique. Before each test, the set of three wafers were stripped and coated with 9 µm thick AZ 10-XT photoresist which is typical for the fan-out process [8]. Details of the photoresist process are described in table 1.

Process Step	Parameters	Equipment
Coat	Static dispense Spin: 1900 rpm for 40 seconds	ACS 200
Softbake	Hotplate, contact 3 minutes at 110°C	ACS 200
Exposure	1000 mJ/cm^2, ghi-line PEB: not required	AP 300
Develop	7 min immersion 2.38% TMAH, 21°C Constant and aggressive agitation DI water rinse Spin rinse and dry	

Table 1. The lithography process used for 9 µm thick AZ10XT photoresist on 200mm substrates.

Since standard overlay measurement structures are not included in the original device, a metrology method was constructed using the vision based alignment system on the stepper. The overlay metrology structure consists of four square features in resist surrounding a cross feature in the device, as shown in figure 2. The coordinates of the resist feature is compared with the device feature to determine offsets in X and Y.

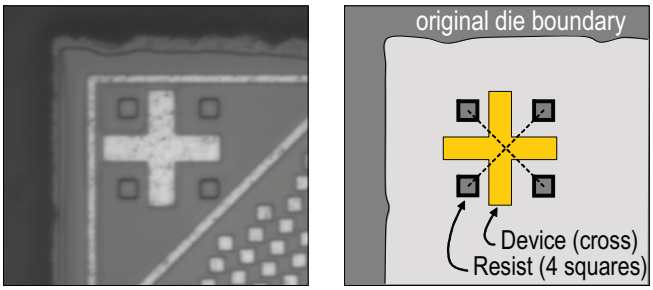

Figure 2. Overlay metrology structure consists of four squares in resist surrounding a metal cross in the device.

Since individual die placement error comprises a large portion of the error budget, a dense sampling strategy was used to characterize this effect. For consistency the metrology sampling included the same 71 points for all alignment strategies, although the stepper field boundaries change between the two die array sizes as shown in figure 3.

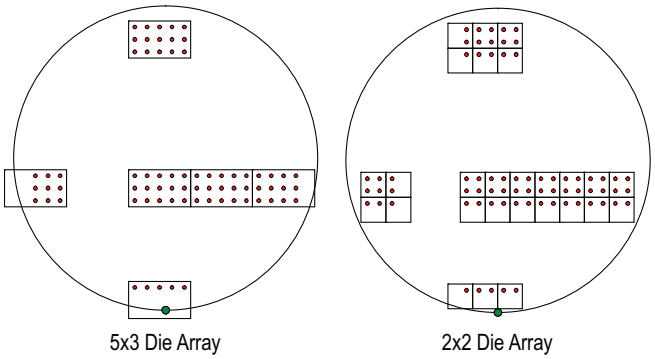

Figure 3. 71 point metrology sampling and relationship to stepper field size for the 5x3 and 2x2 die arrays.

RESULTS AND DISCUSSION

Three fan-out wafers were used for all alignment strategies, measured at the same 71 die locations. The operation of a full wafer aligner was simulated by measuring die positions with an absolute measurement tool after aligning the wafer to the tool using two global alignment marks on the wafer. Stepper operation with various alignment strategies was characterized by measuring the registration of the exposed and developed photoresist pattern to the device die pattern. Prior to each stepper test the wafers were coated with new photoresist.

Figures 4a, 4b and 4c shows registration histograms in X and Y for the full wafer aligner (absolute measurement tool), the stepper using EGA alignment for a 5x3 die array and a 2x2 die array respectively. X registration is shown in blue and Y registration is in red. It is important to note that all data are from the same 3 wafers. Although data from all 390 die on the wafers were available from the absolute measurement tool, only the same 71 locations for the registration tests are used for a consistent comparison.

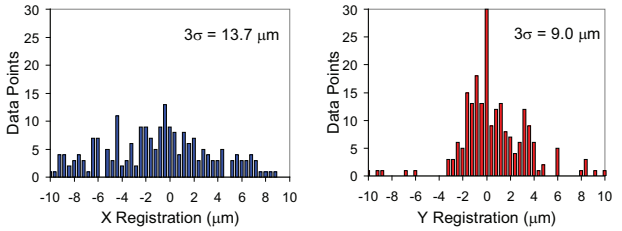

Figure 4a. Registration histograms in X and in Y for the full wafer aligner (absolute measurement tool).

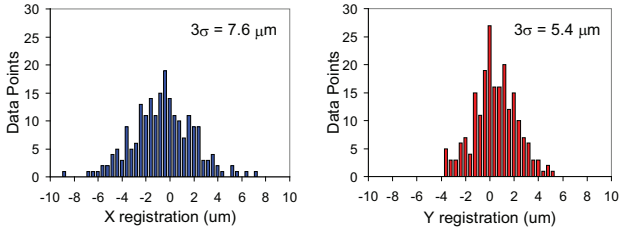

Figure 4b. Registration histograms in X and in Y for the stepper running 5x3 die array EGA alignment.

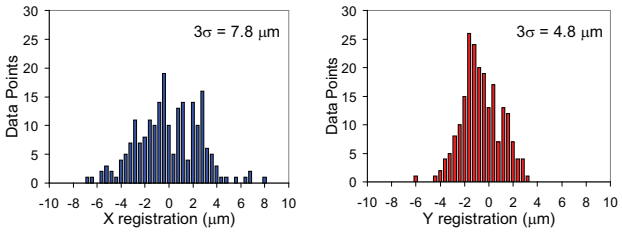

Figure 4c. Registration histograms in X and in Y for the stepper running 2x2 die array EGA alignment.

The registration error distribution is much wider for the full wafer aligner (figure 4a) than for the stepper (figures 4b and c), due in part to wafer-to-wafer mean shifts and mismatch of linear grid terms such as wafer scaling. Since the full wafer aligner operates at fixed scale, any scaling mismatch to the device wafers increases the range of registration error for each wafer. The full wafer aligner has a grid scale mismatch in X of 26, 47, and 54 ppm for the three wafers, indicating considerable wafer scale variation on the fan-out wafers. For stepper EGA operation the linear scaling seen during alignment is automatically adjusted in the run time modeling of shot locations, so even with large die positioning errors scaling error was held below 20 ppm using nine site EGA alignment. Note that since the EGA solution is a modeled fit, the registration is relatively insensitive to stepper field size as shown in figure 4b versus 4c. This is based on the reticle magnification being reasonably well matched to the nominal wafer scale.

Figures 5a, 5b and 5c shows overlay histograms in X and in Y for the full wafer aligner (absolute measurement tool), the stepper running Site-by-Site alignment for a 5x3 die array and a 2x2 die array respectively.

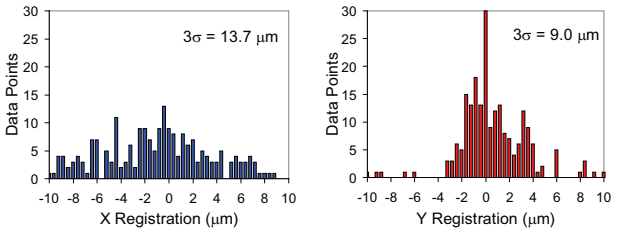

Figure 5a. Registration histograms in X and Y for the full wafer aligner (absolute metrology tool).

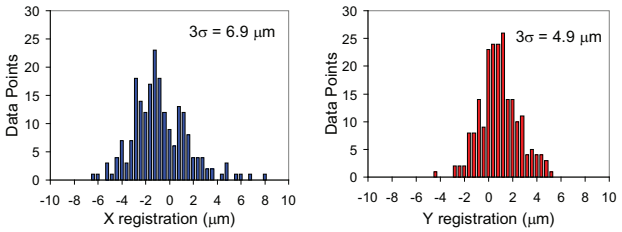

Figure 5b. Registration histograms in X and in Y for the stepper running 5x3 die array site-by-site alignment.

The 2x2 die array (figure 5c) is aligned with a single target per field rather than the standard two targets due to the small

field size. As a result the die containing the alignment mark will show excellent registration compared to the other three die in the exposed array, which explains the sharp central spike in the registration data.

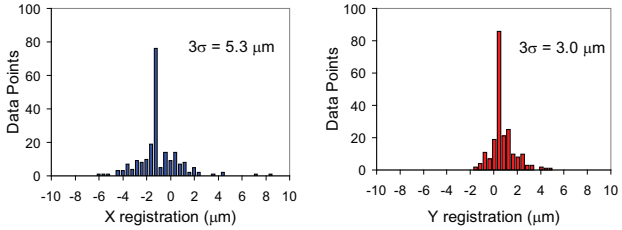

Figure 5c. Registration histograms in X and in Y for the stepper running 2x2 die array site-by-site alignment.

The raw data can be filtered to include only the alignment site die, giving the equivalent of a sparsely sampled 1x1 die array. Registration histograms for the calculated 1x1 die array case are shown in figure 6. This alignment strategy is highly effective in accounting for individual die placement errors. However individually aligning and exposing 390 die on a wafer would have a significant throughput penalty and may not be practical in a production environment.

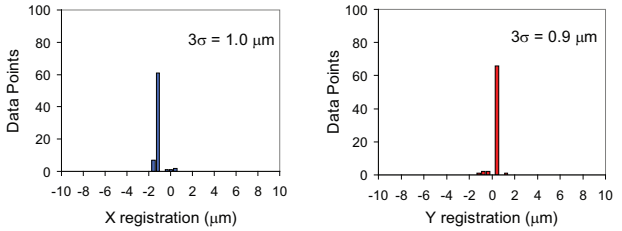

Figure 6. Registration histograms in X and Y for 1x1 die array using stepper Site-by-Site alignment. Narrow distribution indicates that 1x1 die alignment is quite effective in tracking individual die placement errors

Three times the standard deviation or 3 sigma (3σ) is the most common measure of spread for an overlay distribution [5]. The registration 3 sigma for various field size and alignment mode combinations shown in figures 4, 5 and 6 is summarized in figure 7 and table 2. X registration is shown in blue and Y registration is in red.

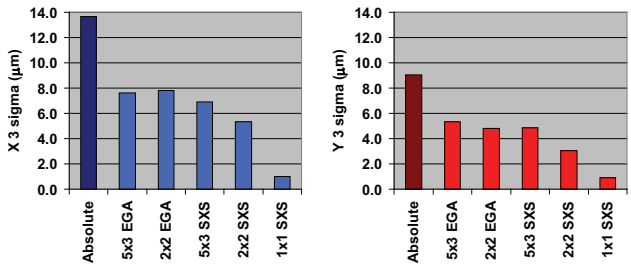

Figure 7. Comparison of full wafer aligner (absolute); stepper EGA and Site-by-Site (SXS) alignment, with three different stepper field sizes (5x3, 2x2 and 1x1). X registration is shown in blue and Y registration is in red.

	Full Wafer Aligner	Stepper 5x3 EGA	Stepper 2x2 EGA	Stepper 5x3 SxS	Stepper 2x2 SxS	Stepper 1x1 SxS
X	13.7	7.6	7.8	6.9	5.3	1.0
Y	9.0	5.4	4.8	4.9	3.0	0.92

Table 2. Comparison of registration 3-sigma (micron) for the full wafer aligner, EGA and Site-by-Site (SxS) alignment on stepper, with different field sizes.

The registration error for the full wafer aligner was approximately 14 µm three sigma. Registration was below 8 µm three sigma for all stepper alignment strategies. At smaller field sizes Site-by-Site gives better overlay than EGA; however at larger field sizes the two alignment modes give comparable overlay. The reason for this convergence is that both EGA mapping and Site-by-Site alignment modes are dominated by die placement error when exposing multiple die. Since EGA and Site-by-Site give similar registration performance at large exposure field sizes, then the faster EGA mode is preferred. This provides for highest productivity and lowest cost per wafer. In addition since EGA is a sampling alignment mode, it has more flexibility for employing alternate alignment sites if primary alignment sites are obscured or damaged. This flexibility is important for maintaining fully automatic operation in high volume manufacturing.

For the die placement errors in this study, fan-out wafers processed on the stepper can achieve significantly better overlay than the full wafer aligner. Both aligner and stepper methods are affected by random die placement errors, however the stepper is better at handling process induced grid variation since it can compensate for linear components of placement error in real time.

CONCLUSIONS

The fan-out wafer die placements can be described by a two dimensional linear grid, subject to die placement error at each grid point. With current fan-out technology, grid parameters such as scaling vary considerably wafer-to-wafer. Therefore, mismatch to a full wafer aligner is considerable due to process variation. Registration improvements to well below 10 µm have been achieved using a stepper exposure tool.

Since the stepper exposes the wafer pattern with multiple shots, scaling can be incorporated by adjusting the stepping positions for each shot. The information needed to make these adjustments can be collected by aligning each shot in Site-by-Site mode, or by sampling multiple EGA alignment sites. Statistically the effect of placement error on measurement of the grid can be minimized by increasing the number of EGA alignment sites. All stepper approaches investigated in this study improved upon the full wafer aligner as simulated from the absolute measurement tool.

The stepper exposure tool offers the potential for further registration improvements by implementing algorithms to

correct linear terms over multiple sub-regions of the wafer rather than across the whole wafer. This would better account for localized die drift across the fan-out wafer. Using this approach would support tighter overlay design rules for multiple generations of fan-out technology for leading edge devices.

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REFERENCES
[1] Gartner Dataquest Semiconductor Briefing, February 2009

[2] Johnson, S., STATS ChipPac to Manufacture Infineon's First-Gen eWLB Products, *Semiconductor International*, August 2008.

[3] Brunnbauer, M. et. al., Embedded Wafer Level Ball Grid Array (eWLB), *Electronics Packaging Technology Conference 8th Proceeding*, December 2006.

[4] Perkins, M. et. al., Intermix technology: The Key to Optimal Stepper Productivity and Cost Efficiency", *Optical/Laser Microlithography V Proceedings*, SPIE **1674** (1992).

[5] Levinson, H., **Principles of Lithography**, SPIE Press, 2001.

[6] Van den Brink, M. et. al., "Performance of a Wafer Stepper with Automatic Intra-die Registration Correction", *Optical Microlithography VI Proceedings*, SPIE **772** (1987).

[7] Todd, B. et. al., "Thick Photoresist Imaging Using a Three Wavelength Exposure Stepper", *Micromachining and Microfabrication Process Proceedings*, SPIE **3874** (1999).

[8] Flack, W. et. al., "Characterization of an Ultra-Thick Positive Photoresist for Electroplating Applications", *Advances in Resist Technology and Processing XX Proceedings*, SPIE **5039** (2003).