Large Area Interposer Lithography

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Abstract

Large area silicon or glass interposers may exceed the maximum imaging field of step and repeat lithography tools. This paper discusses the lithographic process used to create a large area interposer on a stepper by the combination of multiple subfield exposures. Overlay metrology structures are used to confirm the relative placement of the subfields to construct the interposer. Routing lines from 1.5 to 4.0 µm in width are evaluated to measure critical dimension (CD) control where the lines cross the subfield boundaries. CD metrology at the bottom and top of the photoresist is performed using a top down CD-SEM. Finally large area test interposers are patterned using two subfields on a 1X stepper and processed through a Cu electroplating module for detailed characterization.

The CD control of routing lines as they cross the subfield boundary can be optimized by using a shaped or tapered line end design. Lithography simulation using Prolith modeling software by KLA-Tencor is matched to experimental results and then used to evaluate performance of various line end designs. Larger latitude for overlap error was observed for the tapered line end compared to the standard square line end.

The experimental and modeled results in this study show the capability of using stepper lithography to produce large area interposers with 1.5 µm I/O routing line dimensions.

Introduction

Over the last few decades, IC technology has used shrinking gate dimensions to increase gate switching speed and decreased operating voltage to reduce power consumption. As the demand for improved form factor and superior battery life accelerates, the semiconductor manufacturing supply chain is taking a closer look at back end of line (BEOL) manufacturing technology. Innovative IC packaging solutions are being developed to meet the needs in consumer electronics. Furthermore, IC packaging now is widely seen as a method to prolong Moore's law [1]. Many companies are evaluating the use of silicon interposers with through silicon vias (TSV) to address requirements for higher performance and smaller form factor packages. Interposer technology is less complex than full 3D stacking and therefore offers an advantage in time to market. It is currently viewed as the next major step in cost effective advanced packaging technology.

Key advantages of silicon interposers include high routing line density, excellent electrical and thermal performance, lower power requirements than equivalent single-chip packages through combination of multiple chips on one substrate, and the possibility of integrating passives into the substrate [2,3]. The individual device die can provide numerous functions including memory, logic, analog and MEMS (micro-electromechanical systems). Achieving high bandwidth between individual die on the interposer requires fine pitch routing lines. For advanced wide I/O applications, it is anticipated that interconnect line widths of less than 2 µm will be needed.

A step and repeat (stepper) lithography system provides the necessary patterning capability for high resolution devices with zero printable defects. However, for some designs the interposer area can exceed the maximum stepper field size.

Large Interposer Fabrication

The requirement for patterning large area devices with stepper lithography is not new. Superchips from the VHSIC (Very High Speed Integrated Circuit) program were constructed using macrocells [4]. Each macrocell was a self-contained integrated circuit placed in a single stepper field and only interconnect layout rules were used at crossing field boundaries [5, 6]. A more recent demand for large area devices is for infrared focal plane arrays used for aerospace applications [7]. The image sensor pixels are contained within a stepper field and only interconnect routing is allowed to cross stepper field boundaries similar to superchips.

Since interposers are designed to interconnect single chip devices, the field stitching considerations are similar to focal plane arrays and superchips. A large area interposer can be fabricated by splitting the interposer design into multiple sections where each section is smaller than the maximum field size of the step-and-repeat lithography system.

Figure 1 shows a 50 by 50 mm interposer split into a top half (purple) and a bottom half (pink). This two subfield approach would work for a lithography system with a field size greater than 50 by 25 mm.

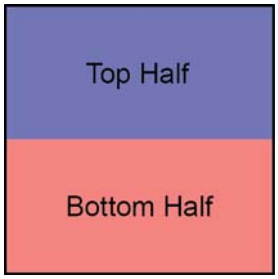


Figure 1. The large area interposer design is split into top and bottom halves for stepper lithography layout.

A reticle for the lithography system is then fabricated for each section of the interposer. Figure 2 shows the layout for a 1x reticle that supports placing multiple fields on one plate. Here the top half of the interposer (purple) is field 1 on the reticle and the bottom half of the interposer (pink) is field 2 on the reticle.

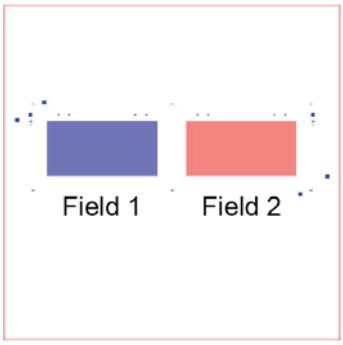


Figure 2. 1X reticle layout for an interposer split into two fields. The reticle size is 150 by 150mm.

This reticle can then be used on the lithography stepper to image the full interposer on the wafer by alternating the patterning of rows of field 1 (purple) and field 2 (pink) as shown in figure 3. The interposer routing lines that cross the boundary of the top half and bottom half of the interposer are stitched by allowing a small amount of Y overlap between the two fields. The same approach could be used to fabricate even larger area interposers by having additional reticle fields stitched in both the X and Y direction. This paper evaluates using this field stitching process to meet the requirements for advanced silicon interposer manufacturing.

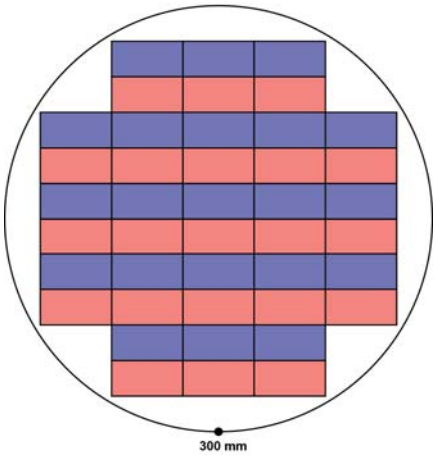


Figure 3. 300mm wafer layout with 21 interposers. The interposer size for this case is 50 by 50 mm.

Experimental Methods

Exposures are performed on an Ultratech AP300 advanced packaging stepper with a 0.16 NA Wynne-Dyson lens [8]. This catadioptric optical system design permits the use of broadband illumination from a mercury arc lamp, and the system used in this study has a capability to select i-line, gh-line or ghi-line wavelengths. The tool is equipped with a WEE (Wafer Edge Exposure) unit for exposing the edge of the wafer and a WEP (Wafer Edge Protection) unit for protecting a predefined outer edge of the wafer. The WEE enables precise removal of photoresist from the wafer edge creating an electrical contact that is required for electroplating. The WEP blocks exposure light and can be used to retain photoresist on a thin ring inside the WEE creating a protective seal ring to prevent leakage of solution during the electroplating step.

The large area interposer evaluated for this study is 44.0 by 44.0 mm with interconnect lines covering the whole chip area. Since the exposure field of the 1X stepper used in this study is 44x26.7mm, the interposer design is split in two fields each with a size of 44 by 22mm similar to figures 1 and 2. The reticle set was designed to include test structures that provide evaluation of overlay and CD performance at the field boundaries. For this case only a Y stitch is required.

Multiple test structures were created to evaluate reticle field stitching performance. Figure 4 shows a line integrity structure with six sets of line and space patterns with varying CD and pitch. The patterns above the red stitch line are on reticle field one and the patterns below the red stitch line are on reticle field two. The CD of the test structures vary from 1.5 µm line and space on the left side to as large as 4.0 µm line and 2.0 µm space on the right. The 0.5 in blue above the pattern indicates that the top and bottom half have a stitch overlap in Y of +0.5 µm between the fields. Additional line integrity structures were created with field stitch overlaps varying from as small as -0.5 µm to as large as +10.0 µm.

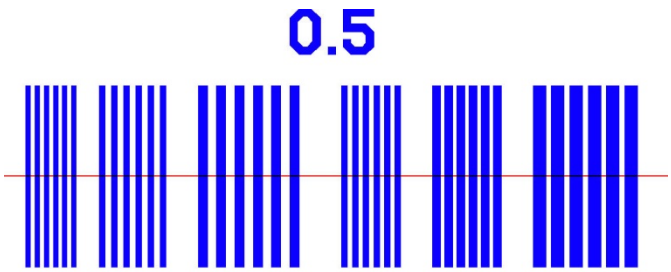


Figure 4. CD performance features with varying pitches. The red line indicates the stitch between field 1 and field 2. The 0.5 above the structure indicates the Y overlap in microns.

An electrical test structure was also created to evaluate the field stitch performance of electroplated Cu lines. Figure 5 shows a serpentine/comb four point probe structure. The pattern above the red stitch line is on reticle field one and the pattern below the red stitch line is on reticle field two. The test structures range from 1.5 µm line and space to 3.0 µm line and space. The field overlap in Y was +0.5 µm.

Initial test of the interposer stitching was performed on bare silicon wafers using JSR IX845 positive tone photo resist. The resultant photoresist structures are evaluated for overlay performance and CD behavior at the stitching

boundary and are used as the reference for the simulation modeling discussed in the "Simulation of Field Stitching" section of this paper.

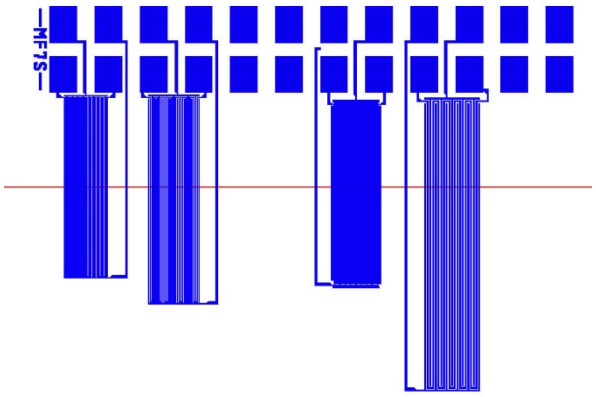


Figure 5. Serpentine/Comb structure. The red line indicates the stitch between field 1 and field 2.

Next the lithographic process was evaluated on Cu seed 200mm wafers using actual device process conditions. The Cu interconnect lines are fabricated using a semi-additive electroplating technique as shown in figure 6. In this technique a Cu seed layer consisting of 30 nm TiW and 50 nm of Cu is deposited on the wafer which acts as the current distributing layer during the electroplating process (figure 6.1). Next a 3.5 µm thick positive photoresist is coated on the wafer and the area to be electroplated is opened to the Cu seed via the lithography process (figure 6.2). The resist is descummed and then 2.5 µm of Cu is electroplated on the wafer (figure 6.3). The photoresist is then stripped off of the wafer (figure 6.4). The Cu seed is wet etched followed by wet etch of the TiW to create the final structure (figure 6.5).

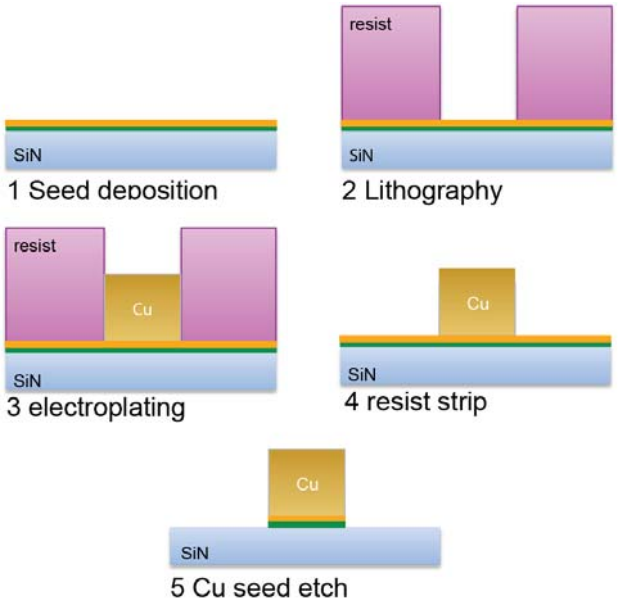


Figure 6. Wafer Process Flow to fabricate Cu interconnect lines using of a semi-additive electroplating technique.

The novolak/diazonaphthoquinone (DNQ) positive tone resist platform is approaching its process limits to adequately meet the demands of advanced packaging applications. DNQ high absorption and low sensitivity impose significant limitations on its resolution, pattern profiles, and photospeed over a wide range of film thickness. Therefore, chemically amplified (CA) resist platforms are believed to be more suitable than (DNQ) platform to fulfill the future needs for advanced packaging applications such as interposers. The higher photospeed of CA resist reduces exposure times and considerably improves the cost of ownership of the lithography tool.

This study employed AZ EXP CN-3 positive resist, which is based on a phenolic polymer, CA platform. This resist can produce vertical sidewalls with minimal footing on Cu substrates, and is capable of resolving submicron patterns in 3.5µm thick resist using i-line lithography. The exposure latitude of 1.5 µm lines and spaces measured on a 0.16 NA stepper was 18% with a ±10% CD criterion.

Processing conditions for AZ EXP CN-3 are summarized in table 1. All resist processing was performed on a TEL ACT12 Clean Track which is equipped with high viscosity pumps for thick resist processing. CD metrology was performed on a KLA 8250XR CD-SEM.

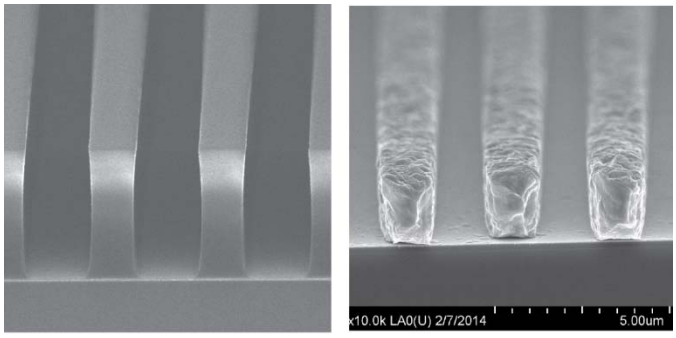
Process Step	Conditions
Soft Bake	120 seconds at 110°C
Post Exposure Bake	60 seconds at 90°C
Development	30 seconds x 2 (double puddle) in 0.26N TMAH developer with surfactant

Table 1. Process conditions used for AZ EXP CN-3 resist.

The 1X stepper offers multiple alignment options, and for this study both blindstep and zero layer alignment were evaluated. Blindstep uses the XY stage encoder along with a previously calibrated transform to accurately print a multiple field array. The zero layer technique requires a dedicated array of field alignment targets to be printed on the wafer. These targets are used to align and stitch two adjacent reticle fields together to optimize overlay. Overlay metrology was performed using microscope measurements and using the self-metrology feature on the 1X stepper.

Results

For this study the AZ EXP CN-3 resist was exposed at i-line using a nominal exposure dose of 140 mJ/cm^2 . The resist was optimized to produce a 1.5 µm line and space pitch on Cu seed wafers. A cross section of 3.5 µm thick AZ EXP CN3 photoresist is shown in figure 7(a). The resist exhibits an excellent profile with minimal footing. Cross sections of Cu plated lines are shown in figure 7(b).

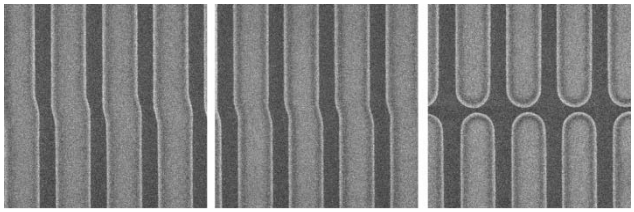


(a) AZ CN3 Resist (b) Cu Plated Lines

Figure 7. (a) Cross section of 3.5 µm thick AZ EXP CN3 photoresist. The exposure dose is 140 mJ/cm^2 and the focus

offset is 0 µm. (b) Cross section of Cu plated metal lines before Cu seed etch. Both cases are for line and space pattern with 3 µm pitch.

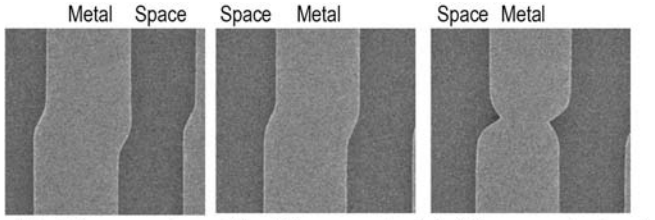
Sample interposer structures were stitched together using two lithography fields. The resist line at the stitch area was evaluated for three different Y axial offsets (overlap). Figure 8(a) shows a positive overlap of 1.0 µm and the positive resist line at the stitch decreases in CD. Figure 8(c) shows a negative overlap of 0.5 µm and the resist line bulges out and merges with adjacent lines. Note that these images are taken before the descum step which would further open the spaces between resist lines.



(a) Overlap of +1.0 µm (b) Overlap of +0.5 µm (c) Overlap of -0.5 µm

Figure 8. Effect of Y overlap at the stitch of resist spaces for a 3 µm pitch structure. The resist feature is dark in these images. The lateral offset is 0.25 µm. These images are taken before the resist descum process.

The effect of the Y overlap was also evaluated after Cu electroplating. Figure 9 shows three cases: (a) 1.0 µm overlap, (b) 0.5 µm overlap, (c) -0.5 µm overlap (a gap). A large overlap creates a bulge in the line at the stitch whereas a gap creates a line constriction. Taken to the extreme, a large overlap can create an electrical short and a large gap can create and electrical open. Therefore to preserve line integrity the Y overlap error must be controlled. Based on these experimental results a 0.5 µm overlap is used in the rest of this study.

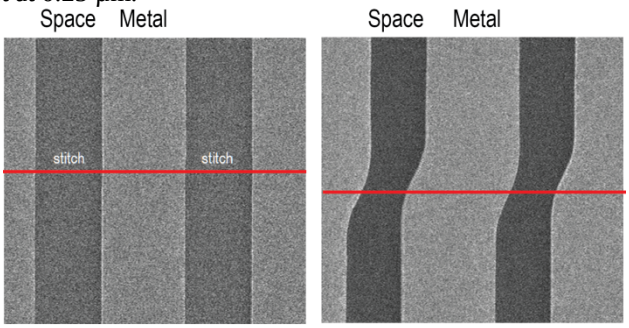


(a) +1.0 µm overlap (b) +0.5 µm overlap (c) -0.5 µm overlap (gap)

Figure 9. Effect of Y axial offset at the stitch for plated metal lines for a 3 µm pitch structure.

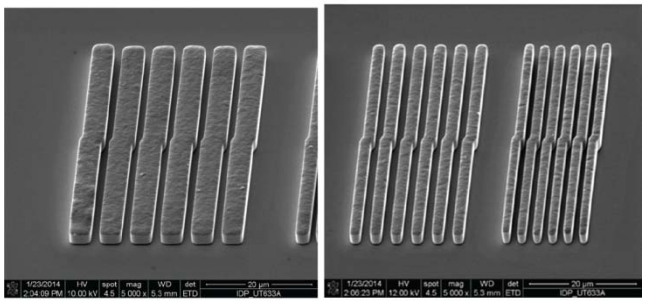
Figure 10(a) shows a top down SEM of stitched dense plated lines with 3 µm pitch. The plated lines form within the spaces of the resist pattern. This view shows an optimized stitch for which the actual stitch location is difficult to discern. A red horizontal line is added to the stitch location. For instructive purposes it is useful to include moderate amounts of lateral offset in the stitch in order to clearly denote its position. Figure 10(b) shows stitched plated line with a large lateral offset of 0.5 µm. With large lateral offset the line is well defined and maintains adequate width, however the spaces between the lines become constricted.

Tilted SEM images of the plated lines are shown in figure 11(a) and 11(b). The images illustrate ability to fabricate line/space metal lines down to the 1.5 µm and to stitch these lines across a field boundary. In this case the lateral offset was set at 0.25 µm.



(a) No lateral offset (b) Lateral offset of 0.5 µm

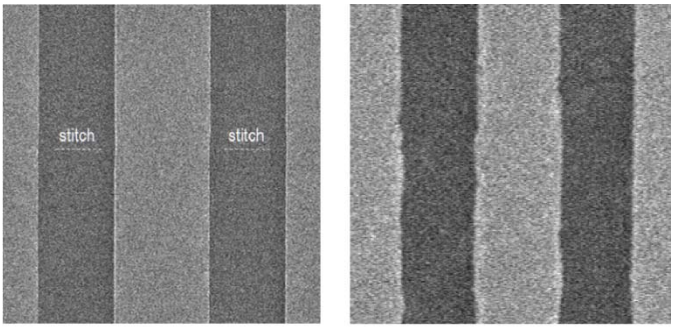
Figure 10. Stitched plated metal lines at 3 µm pitch with (a) no lateral offset and (b) a lateral offset of 0.5 µm. The overlap is 0.5 µm. The red line is the field stitch location.



(a) Pitch = 6 µm (b) Pitch = 4 µm and 3 µm

Figure 11. Electroplated metal lines at stitch with (a) 4 µm line and 2 µm space and (b) 4 µm and 3 µm pitches equal line and space pitches. Both cases have a lateral offset of 0.25 µm.

The steps following resist development also influence the shape and size of the Cu lines. Both descum and the seed removal steps need to be optimized for effective control of CD. Descum is essential for uniform plating results because it reduces the surface tension of the photoresist to allow proper wetting to the Cu seed. However, this process consumes photoresist and the CD of the resist opening increases as a result. Figure 11(a) shows one line exhibiting some non-uniformity which indicates that the descum is on the limit of being too soft.



(a) Before Cu seed etch (b) After Cu seed etch

Figure 12. Top down view of Cu plated metal lines (a) before Cu seed etch and (b) after seed etch. Both cases are for 3 µm pitch, line and space pattern.

The seed etch also can have a large impact on the shape and size of the Cu lines. During wet etching of the Cu seed, the electroplated structures are also etched with a reduction of

CD as a result as shown in Figure 12. To reduce this effect the Cu seed thickness needs to be as thin as possible in order to minimize the etching time. For example, using a standard Cu seed thickness of 150nm results in more than 400 nm CD loss, which would be unacceptable for creating 1.5 µm Cu lines. This is the reason that a 50nm Cu seed was used in this study.

Figure 13 shows top down view of a Cu electroplated serpentine/comb structure with a 3µm pitch. Visual inspection reveals no line breaks or shorts in any of the serpentine/comb structures. Future work includes electrical characterization of these four point probe structures.

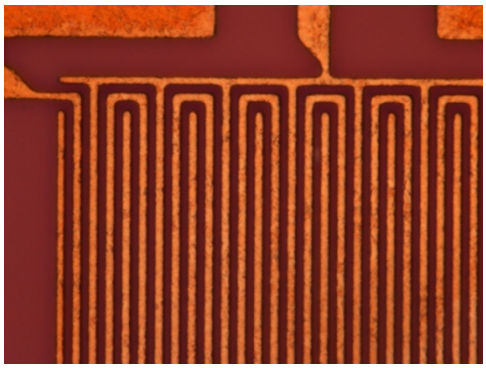


Figure 13. Cu electroplated serpentine/comb structure with a 3 µm pitch. Visual inspection reveals no line breaks or shorts in the structure.

Simulation of Field Stitching

A lithography simulation program (Prolith version 14.1.1.1 from KLA-Tencor) was used to study the effect of stitching overlap and lateral offset on the resist pattern for stitched vertical lines. The pattern consists of 1.5 µm dense vertical lines. Two photomask passes are used to accurately simulate the separate top and bottom field exposures. Figure 14 illustrates the construction of the Prolith model for a standard square corner line end.

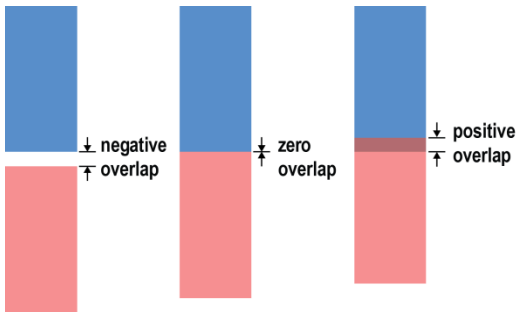


Figure 14. Simulation conditions for stitching line with square ends with lateral offset and overlap. The top and bottom exposures are independently simulated.

The construction of a tapered line end is shown in figure 15. The objective is to determine whether changing the shape of the line ends from square ends can improve process margin for misalignment. For the square line ends the zero overlap condition is defined where the two line ends just meet. For the tapered line ends the zero overlap is defined where the full width shoulders of the tapers meet. In both cases, a positive overlap moves the bottom feature up in Y relative to the top feature. For lateral offset a positive shift moves the bottom feature to the right in X relative to the top feature.

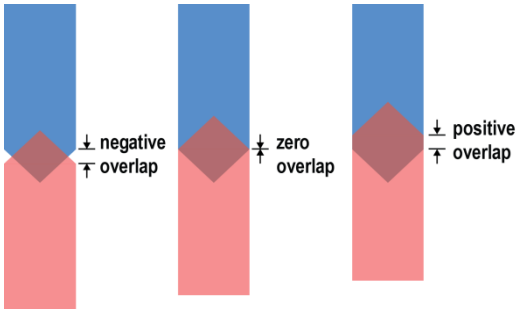


Figure 15. Simulation conditions for stitching line with 45 degree tapered ends with lateral offset and overlap.

Experimental test patterns were exposed in 2.7 µm thick JSR IX845 resist on a 200 mm wafer, and SEM photos were taken to document resist performance at the stitch for different offsets. Figure 16(a) shows top down SEM of a stitch with measured X and Y offset of 0.2 and 0.75 µm respectively. The corresponding figure 16(b) shows a Prolith 3-dimensional resist simulation of the same conditions. Note the resist feature is grey in this figure. Experimental and simulated results show very good agreement, which gives confidence in using modeling to investigate the effect of stitching overlap and lateral offset on line quality.

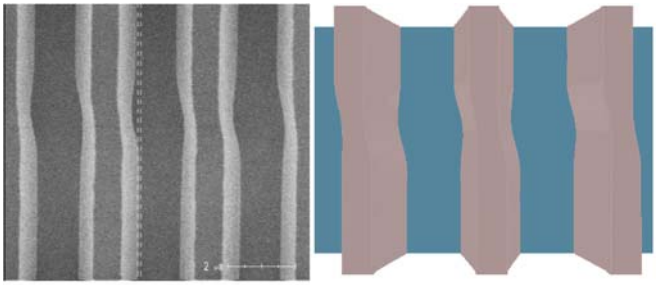


Figure 16. 1.5 µm stitched lines with lateral offset of 0.2 µm and overlap of 0.75 µm. (a) Top down SEM of resist pattern. (b) Prolith simulation of the resist pattern with square ends.

To minimize the CD variation across the stitch a reasonable starting goal is to hold the lateral offset to 20% of the line width. For 1.5 µm line/space this translates into a ±0.3 µm offset range. A similar number can be used for the overlap range. Prolith simulation was used to determine the effectiveness of these criteria for stitched lines.

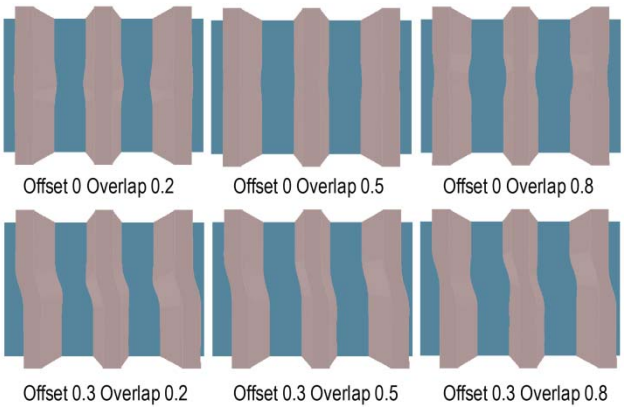


Figure 17. Square end stitch simulation of 1.5 µm lines with overlaps varying from 0.2 µm to 0.8 µm and lateral offsets of 0.0 (top row) and 0.3 µm (bottom row).

Figure 17 shows a sequence of simulations for different values of overlap and lateral offset for square line ends. Overlap range shown in figure 17 is 0.2 to 0.8 µm. Note that resist feature is grey in this figure. CD at the stitch is well controlled, however one can see that as overlap decreases, the resist line starts to bulge at the stitch; and with increasing overlap, the resist line constricts. The effect of a lateral offset of 0.3 µm is shown in the bottom row. For large lateral offsets the rotation of the dense lines at the stitch reduces the spacing between adjacent lines. Both overlap and lateral offset need to be controlled in order to maintain line integrity across the stitch. However the overlap parameter has the larger effect on CD at the stitch.

The effect of tapering the line ends was studied using simulation. A 45 degree taper ending in a point was investigated. For this end shape, the definition of zero overlap is where the full width bases of the tapered lines meet. Prolith simulations show a range of overlap from -0.5 to 0.1 µm where linewidth is moderately well controlled as shown in figure 18. The effect of a lateral offset of 0.3 µm is shown in the bottom row. The stitched lines with tapered line ends have smoother transitions than the stitched lines with square line ends.

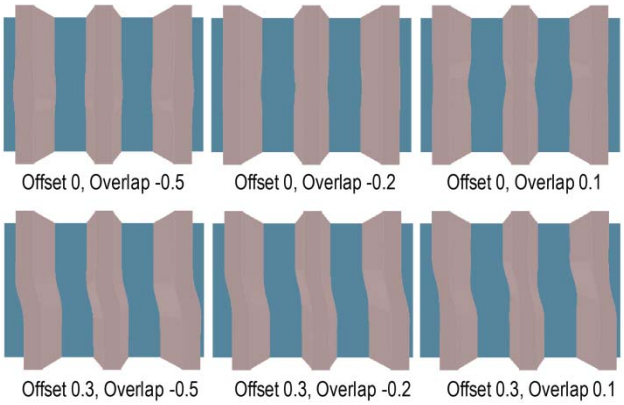


Figure 18. Tapered ends stitch simulation of 1.5 µm lines with overlaps varying from -0.5 µm to +0.1 µm and lateral offsets of 0.0 (top row) and 0.3 µm (bottom row).

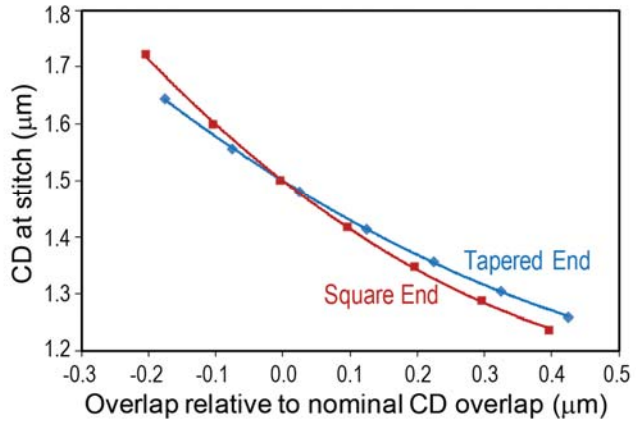


Figure 19. Comparison of resist line CD versus overlap for square and tapered line ends. Data from Prolith modeling of JSR IX845 resist. Overlap scale is shifted so that zero overlap corresponds to the condition where CD at the stitch equals the nominal linewidth of 1.5 µm.

The resist linewidth at the simulated stitch was measured for various overlaps, with zero lateral offset as shown in figure 19. For both square and tapered line end types the CD versus overlap behavior can be well described by a quadratic fit. For comparison between square and tapered line ends the overlap is shifted such that zero overlap corresponds to the condition where the CD at the stitch equals the nominal linewidth of 1.5 µm. The nominal CD is obtained at an overlap of 0.41 µm for the square ends and -0.32 µm for the tapered ends. It is apparent that the slope of the tapered end curve is less than the square end curve, indicating larger latitude for overlap error for the tapered end. If a ±10% CD tolerance is allowed the overlap range is 25% larger for the tapered line end relative to the square line end.

The resist model based on JSR IX845 resist characteristics can be compared to actual measured CD data using AZ EXP CN-3 resist. Note that these measurements are of the space between resist lines, since the space defines the size of the plated lines. Figure 20 shows the 1.5 µm resist features on a 3.0 µm pitch with 0.3 µm and 0.8 µm overlap. Here the total overlap is calculated by adding the design overlap and the measured registration at the stitch site. The CD at the stitching line is measured and compared to the "nominal" CD just above and below the stitching line. At 0.3 µm overlap the CD of the space is 342 nm smaller than nominal and at 0.8 µm the CD of the space is 256 nm larger than nominal. The estimated optimum CD at the stitch occurs at 0.59 µm overlap based on linear interpolation, or 0.55 µm based on fitting to the curvature in figure 19 for square end lines. The experimental data for AZ EXP CN-3 resist shows a reasonably good fit to the model. Further experiments would be needed to fine tune the model specifically for AZ EXP CN-3 resist.

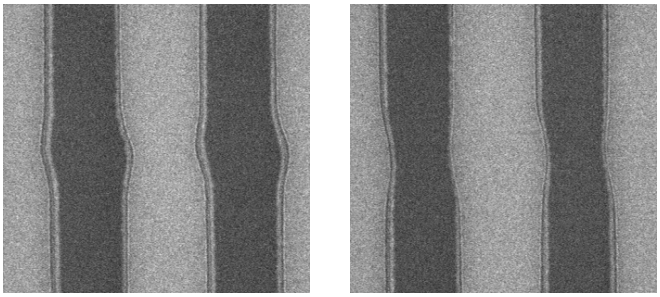


Figure 20. AZ EXP CN-3 resist lines (dark features) at stitch. 1.5 µm CD lines and spaces across the stitching line for +0.3 and+0.8 µm overlap. Lateral offset is 0.1 µm.

Conclusions

Extending device performance increasingly relies on advancements in back end technologies such as the use of very large interposer designs with aggressive interconnect density requirements. A stepper system provides the necessary patterning capability for high resolution devices with zero printable defects. However to produce large area interposers requires stitching of stepper subfields.

This study experimentally investigated patterning copper lines with lateral dimensions as small as 1.5 µm line/space in a vertically stitched 44 by 44 mm device. To achieve this an experimental AZ EXP CN-3 resist was employed. The resist must meet a combination of requirements for this application

including high resolution, steep sidewalls and chemical resistance to the Cu electroplating process.

Lithography simulation was used to further study the line fidelity across the subfield boundary, including the effect of stitching error and effect of changing the line end shape at the stitch. Larger latitude for overlap error was observed for the tapered line end compared to the standard square line end. This characterization is useful for improving process control of the lithography step.

This work demonstrates that stitching of subfields for interposer interconnects can be achieved by leveraging existing stepper lithography and processes technologies.

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