

OPTIMIZATION OF THROUGH SI VIA LAST LITHOGRAPHY FOR 3D PACKAGING

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ABSTRACT

In this paper we optimize the back-to-front overlay of Through Silicon Via (TSV) patterning for a 5 μm via last process. After TSV patterning, overlay verification poses a challenge because the reference layer is buried underneath the thinned silicon wafer. For both back-to-front alignment and verification a wafer stepper equipped with a Dual Side Alignment (DSA) system is used. The stepper has a self-metrology capability to measure back-to-front overlay at any location on the wafer and model the acquired data using industry standard lithographic error analysis techniques to enable insight into the overlay performance.

The experimental wafers are fabricated by patterning the first interconnect metallization of a TSV-last test chip designed for process characterization. The wafers are then temporarily bonded to a carrier and thinned to 50 μm . The final process step is chemical mechanical polish (CMP) of the silicon surface. In order to investigate the overlay performance, Stepper Self Metrology (SSM) is performed at the four corners and the center of the lithography field. Multiple lithography fields per wafer and multiple wafers are measured to obtain a statistically significant data set for overlay analysis.

Overlay verification is performed by dedicated software on the lithography system utilizing the DSA alignment system. The image capture determines the offset between the TSV photoresist pattern and the reference metal pattern buried under the thinned silicon wafer. Tool Induced Shift is characterized and included in the measurement routine. The verification software provides a data summary and alignment correctable variables to optimize the via-last overlay. It was observed that non-linear effects from the incoming wafers in this study were a limiting factor in the achievable overlay performance. On good quality wafers the overlay performance is better than 750nm which meets the requirements for 5 μm diameter TSV's.

Key words: TSV Last, Via last, Metrology, Overlay, back-to-front side alignment, 3D Integration

INTRODUCTION

Leading edge device manufacturers and foundry customers are evaluating use of TSV to enable next generation 3D Packaging. The common methods for TSV packaging include via first, via middle and via last process flows. Via last is a wafer backside approach that provides extensive flexibility since the process can be implemented at either the foundry or OSAT manufacturing location. The associated Re-Distribution Layers (RDL) for TSV-last can be formed using a traditional Damascene style approach, which ensures a well controlled and common process across many different manufacturing facilities. TSV-last processing is similar to TSV-middle in that a large via is formed which requires the deposition of a liner and barrier followed by complete filling and planarization. However, TSV-last processing removes potential interference of the large TSV's with Back End of Line (BEOL) processing. Additionally the TSV-last approach is complimentary to the continuation of scaling for the non-TSV elements of the process flow such as wafer to wafer bonding accuracy.

Lithography is one of the critical factors affecting overall device performance and yield for via last TSV fabrication [1]. Scaling the diameter of the TSV is a major driver for improvement in system performance and cost. Current via last diameters are approximately 30 μm and are being scaled to 5 μm . There is the potential to further decrease via diameters to less than 2 μm . One of the unique lithography requirements for via last patterning is the need for back-to-front side wafer alignment. With smaller TSV diameters, the back-to-front overlay becomes a critical parameter because via landing pads on the first level metal must be large enough to include both TSV critical dimension (CD) and overlay variations. Reducing the size of via landing pads provide significant advantages for device design and final chip size.

The manufacturing approach utilizing three dimensional (3D) TSV technology alleviates interconnect delay considerations by reducing global interconnect wiring length. In addition, TSV technology enables superior bandwidth performance, improves power management and

addresses some device latency issues. Many companies have research activities in 3D TSV technology and numerous demonstration vehicles have been developed [2,3]. Some of these TSV process sequences require the need for back-to-front alignment solutions during the lithography process step.

Interposers for packaging also require TSV technology. Devices under consideration for use with interposers include graphics processors, high-end ASICs, and FPGAs. The drivers are mainly partitioning large die, integrating single chips into a module, reducing die size where substrate density is the constraint, and the use of the interposer to minimize the stress on large die that is fabricated with extra-low-k dielectrics (ELK).

While image sensors have utilized TSV technology in mass production over the last few years, it is projected that DRAM manufacturers will begin utilizing the TSV packaging technology within several years [3,4]. Adoption of this technology by memory companies can play a significant role in driving technology forward. However the requirements for memory manufacturers are much more stringent and require development of improved back-to-front alignment capability.

ALIGNMENT SYSTEM

The naming convention used in this study is that the wafer device side is the front side and the silicon side is the back side. The side facing up on the lithography tool is the back side of the TSV wafer as shown in figure 1.

Various methods have been investigated for viewing embedded lithography alignment targets [5,6,7]. The method of top IR illumination, shown in figure 1, provides practical advantages for integration with stepper lithography. Since the illumination and imaging are directed from the top, this method does not interfere with the design of the wafer chuck, and does not constrain alignment target positioning on the wafer.

The top IR alignment method illuminates the alignment target from back side using an IR wavelength that can transmit through silicon (shown as light green in figure 1) and the process films (shown in blue). For this configuration the target (shown in orange) needs to be made from an IR reflective material such as metal for best contrast. The alignment sequence requires that the wafer move in Z in order to shift alignment focus from the wafer surface to the embedded target.

The lithography system used in this investigation has a top IR alignment system that supports back-to-front side alignment applications. The back-to-front side alignment or dual side alignment application was originally developed for CMOS image sensor applications [4]. This application required alignment to embedded metal targets below silicon, and the second generation DSA system was designed to achieve back-to-front side overlay of less than 1.0 μ m

($|\text{mean}| + 3\sigma$) over a full 300mm wafer. However, a large portion of this budget is consumed by the error uncertainty of the back-to-front metrology [6,8].

Unlike many front side alignment systems which view the wafer through the projection lens (TTL), the DSA alignment system views the wafer in an off-axis configuration. Therefore the calibrated offset between the exposure and alignment systems is maintained using a common stage fiducial that is measured by both the DSA and TTL alignment systems. Note that the DSA alignment camera is in a fixed position. The wafer stage on the stepper moves in X and Y to enable alignment at any location on the wafer, and the wafer stage also provides the range of Z travel to allow focus on both top surface targets and embedded targets across the practical range of silicon thicknesses.

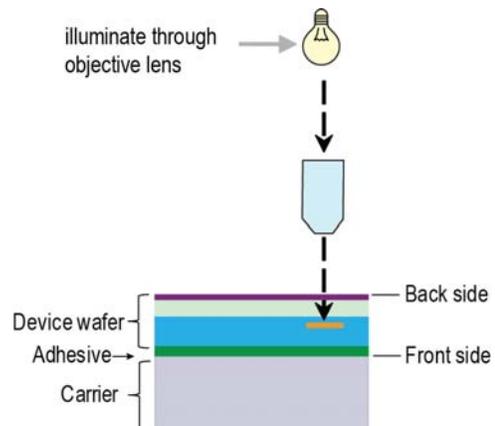


Figure 1: Off axis alignment configuration with infrared illumination and imaging from above the wafer. This configuration is extremely flexible, providing access to the entire wafer for target alignment.

METROLOGY

To eliminate the inherent restrictions in topside planar metrology, a direct, back-to-front side registration metrology package was developed to run on the lithography system, utilizing the off-axis IR alignment system. A dedicated software option was developed to capture both reference patterns and TSV patterns at pre-programmed locations inside the die, and on all dies of the wafer.

As observed in figure 2, the reference feature and the resist feature are not in the same focal plane and it is not possible for both features to be accurately captured with one focal setting. For a silicon thickness of 50 μ m, focusing on one feature will make the other feature out of focus. Therefore, each feature must have its own focus offset to be programmed in the measurement recipe. The image capture system then identifies the relative location of both patterns to determine possible offsets. When the wafer, or batch of wafers, is completely measured the software will analyze the offsets and use a stepper overlay model to determine stepper correctable offsets.

The concept of Tool Induced Shift (TIS) provides a method to compensate for systematic measurement errors. The basic

idea is that two measurements taken at 0 and 180 degree wafer orientations can be represented as two components of error (1) a TIS error component which is independent of orientation, and (2) a characteristic or “actual” measurement which rotates with the wafer. Since tilt between the wafer and measurement tool is a source of TIS, the extent and composition of films in the optical path can modulate TIS, and in practice the measured TIS error may have a process dependency. However for well controlled processes having consistent TIS measurements, the TIS concept provides an effective method for correction of data.

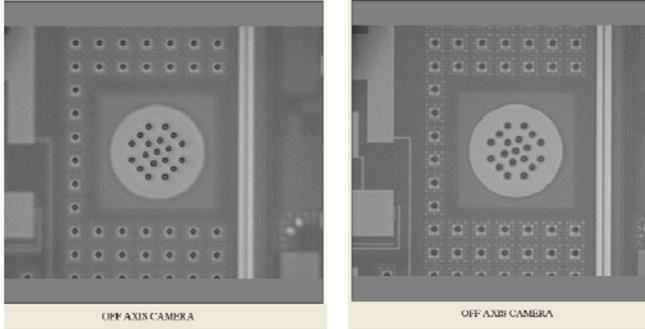


Figure 2: Left-hand image shows the resist target (a cluster of TSV’s) in focus. These are on the top surface. The right-hand image shows the big circle of METAL1 in focus. The dummy patterns of the BEOL are now in focus. The height difference between the two is larger than the focal depth of the alignment camera so always one of the two is out of focus.

Tool Induced Shift

Non-symmetric illumination, tilting of the wafer, tilting of the DSA camera, or photoresist processing effects may introduce TIS [9,6]. This error component is typically measured once for every batch of wafers by an extra measurement of one wafer rotated over 180°. Comparing the data set when measured normally with the 180° will reveal actual overlay offsets and the TIS.

The basic TIS calculations are summarized in equations (1) through (4) [9]. Subscript “0” denotes zero degree orientation measurement, and “180” denotes 180 degree orientation measurement.

$$TIS_x = \frac{X_0 + X_{180}}{2} \quad (1)$$

$$TIS_y = \frac{Y_0 + Y_{180}}{2} \quad (2)$$

$$X_{0,corrected} = \frac{X_0 - X_{180}}{2} \quad (3)$$

$$Y_{0,corrected} = \frac{Y_0 - Y_{180}}{2} \quad (4)$$

Figure 3 depicts a visualization of the two components involved. The apparent error is the vector sum of the actual error and the TIS. To obtain the actual error requires removal of the TIS component from the measurement data.

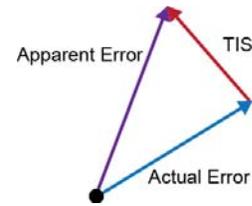


Figure 3: The apparent error (raw measurement) shown in purple is the sum of actual error shown in blue and TIS shown in red.

Rotating the wafer by 180 degrees will reveal a dataset consisting of inverted actual data combined with unchanged TIS. Vector algebra then leads to formulas 1 through 4, identified previously. Figures 4 and 5 illustrate these calculations. Adding the 0 degree and 180 degree datasets gives twice the TIS, and subtracting gives twice the actual data.

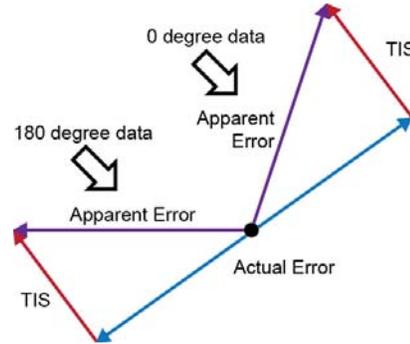


Figure 4: For a 180 degree rotation of the wafer the error associated with the wafer rotates, but the TIS component is stationary.

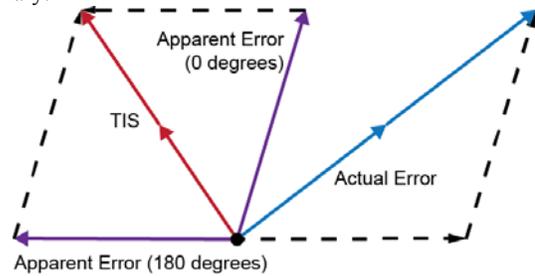


Figure 5: The actual error can now be determined from the difference between the 0 and 180 degree measurement, and the TIS can be determined from the sum.

Wafer rotation and TIS site locations

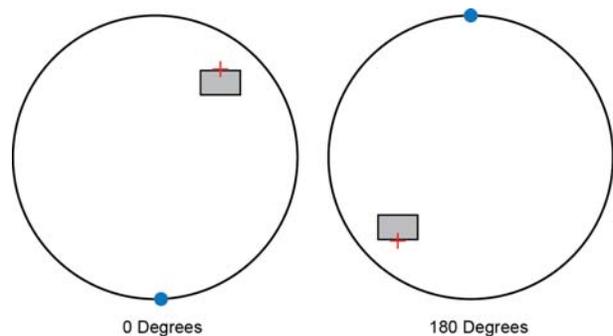


Figure 6: Movement of step position for 180 degree rotation. The blue dot indicates the wafer notch.

To locate corresponding sites on the wafer layout after 180 degree rotation requires rotating the layout. A 180 degree rotation is equivalent to a sign flip for both X and Y coordinates. Figure 6 shows the motion of a point after 180 degree wafer rotation. Using wafer layout information from the process job, the DSA-SSM software can automatically locate the corresponding measurement points for both 0 and 180 degree rotation. This enables measurement of many points on a wafer and multiple wafers to provide the detail needed to perform overlay optimization.

EXPERIMENTAL METHODS

Test Vehicle

All processing is performed on 300mm wafers with damascene METAL1, temporary bonding, grinding and a final surface finish by CMP. Figure 7 depicts a representation of the complete process flow including TSV etch, TSV fill, RDL and de-bonding from carrier. The TSV diameter is 5 μ m and the silicon thickness is 50 μ m, which is typically denoted as a 5 x 50 μ m TSV process. Alignment requirement is that the TSV etching will land completely on METAL1 pads (blue). This paper investigates the image placement after TSV litho, which occurs before the TSV etch and filling. For 5 μ m TSV's an overlay performance of less than 750nm would be required. Although this study evaluated 5 μ m TSV's the mask set supports TSV sizes down to 2 μ m.

Two photo-resists were examined in the experiments: 1) a gh-line novolak based resist requiring 1250mJ/cm² exposure dose and 2) an i-line Chemical Amplified Resist (CAR) requiring 450mJ/cm². Thickness of both materials is tuned to 7.5 μ m. The pattern defined by the TSV lithography is a 5 μ m via.

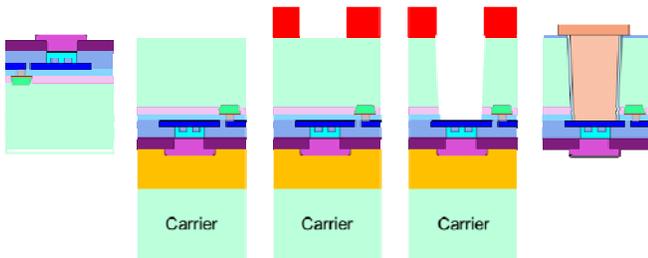


Figure 7: Representation of complete TSV-last process. From left to right: 1) Front-end and Back-end processing, 2) Temporary bonding and thinning, 3) TSV-last lithography, 4) TSV etch, 5) TSV filling, RDL and de-bonding from carrier.

For TSV-last process development a reticle set was made that includes verification features for SSM at 5 locations in the die (depicted in figure 8). The DSA alignment features are located along the top die edge and are of a type reported in [5,7]. The features for DSA-SSM verification are bound by process integration requirements. TSV etching is performed by Bosch etching [1]. For process fidelity the TSV's must land on a METAL1 pad. Because this process is very sensitive to pattern size and density, the vias defining the TSV's are restricted to one type and one size [7]. This dictates that the DSA-SSM features for TSV alignment must

be constructed from a suitable cluster of TSV's. The design for DSA-SSM overlay features for 5 μ m diameter TSV is depicted in figure 9. This cluster is designed with unique grouping and rotation that create isolation from device TSV's and thwart incorrect selection during alignment and capture.

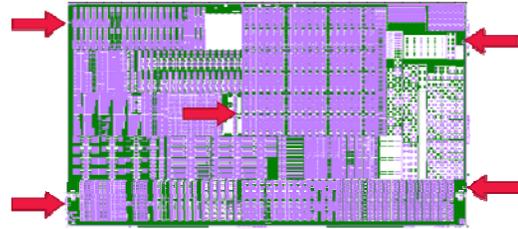


Figure 8: TSV-last process development reticle. The red arrows indicate DSA-SSM overlay verification locations. This pattern is flipped when viewed from the back side.

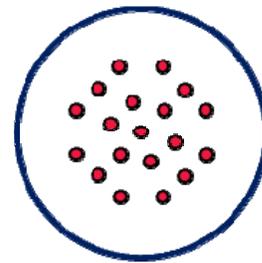


Figure 9: DSA-SSM overlay feature for 5 μ m diameter TSV's. The blue ring indicates the landing pad in METAL1 which is the reference layer. The cluster of red circles is printed in the photoresist. A photograph of this structure is shown in figure 2.

RESULTS AND DISCUSSION

Repeatability

To characterize the repeatability of the DSA-SSM measurement, each die on the wafer (115 die per wafer) was measured 5 separate times. Repeatability is shown in figure 10. Average 3 σ is 30nm in X and Y. This is within the requirements for less than 750 nm overlay performance of this process.

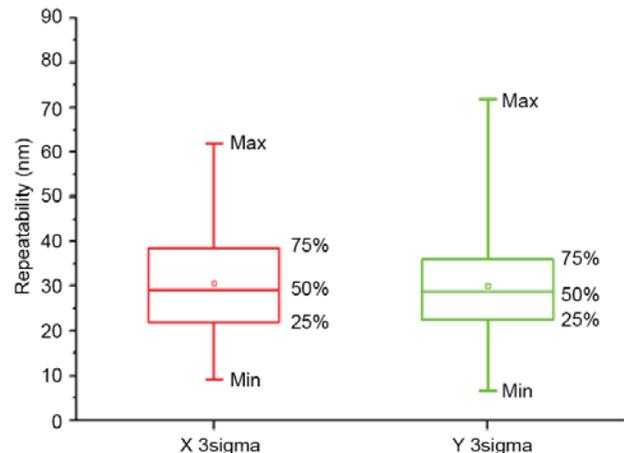


Figure 10: Repeatability of DSA-SSM measurement for a single wafer measured multiple times at 115 points. Each point on the wafer is measured 5 times to calculate 3 σ for each point. Average 3 σ is 30 nm in X and Y.

Calculation of TIS

Tool Induced Shift was characterized by measuring at 0 and 180 degree orientations and then analyzing the data. Figure 11 shows a vector plot example of a 0 degree measurement and 180 degree measurement of the same wafer. The sum of offsets for the two orientations divided by 2 gives the TIS estimate. The average TIS offset is -155nm and -453nm for X and Y respectively. For comparison purposes the 180 degree wafer map, in figure 11, is a composite which combines the measurement sites for the 0 degree layout, with the measurements taken at 180 degree.

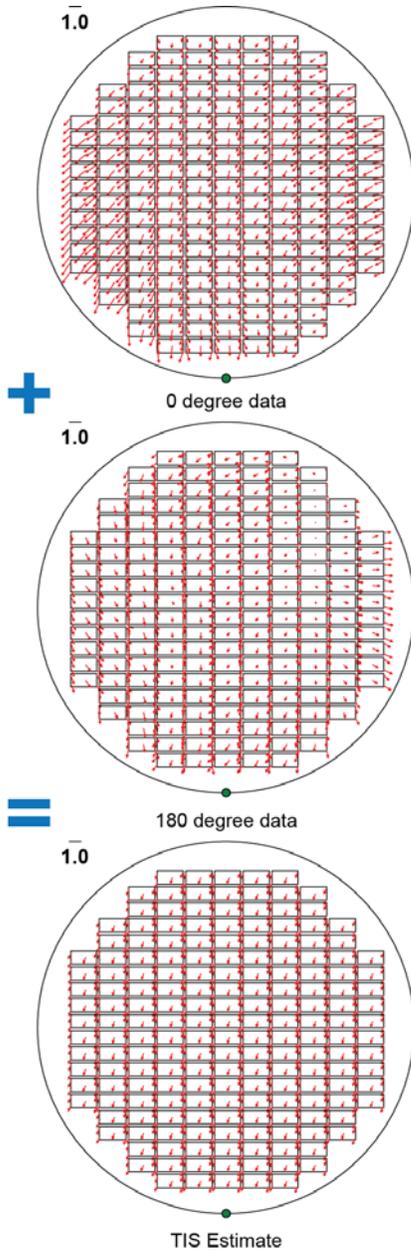


Figure 11: Calculation of TIS estimate from 0 degree and 180 degree measurements using equations 1 and 2. For ease of visual comparison, both sets of measurements are plotted on the original 0 degree layout map.

Corrected Measurements

The TIS component of the measurement needs to be subtracted out in order to get a corrected measurement useful for process evaluation. The corrected measurement can be obtained by subtraction of offsets for the two orientations at corresponding points and dividing by 2, as shown in figure 12.

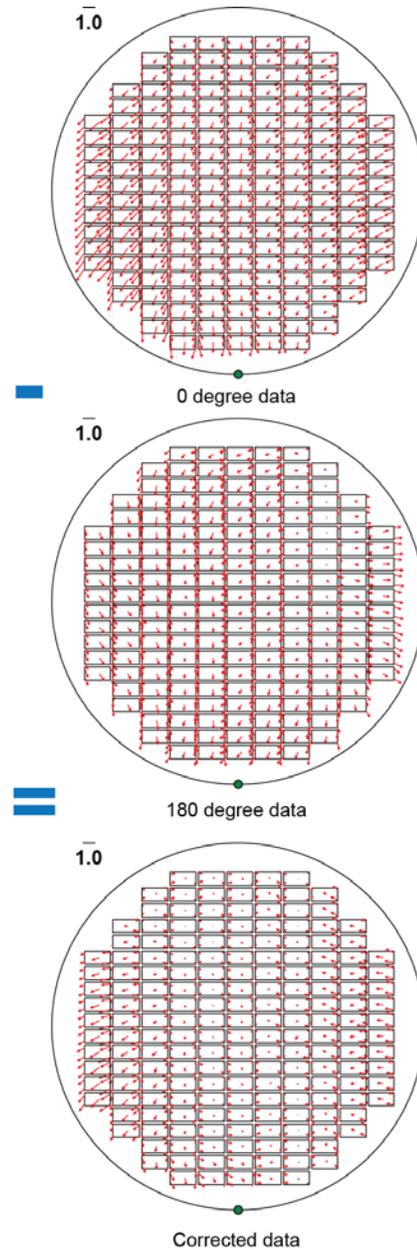


Figure 12: Calculation of Corrected data from 0 degree and 180 degree measurements using equations 3 and 4. The wafer 3σ is $0.859\ \mu\text{m}$ in X and $0.543\ \mu\text{m}$ in Y.

The TIS estimate is uniform across the wafer and the corrected data has a smooth variation consistent with physical error sources. Since the TIS values are consistent, a single TIS mean correction can be used to correct the mean for the 0 degree run.

Two sampling plans were used in this investigation. The dense 920 point sampling plan, shown in figure 13(a), measures 184 steps and provides detailed information which can be used to improve parameter estimation and to investigate higher order terms. For routine process monitoring, fewer points are required, and a 115 point sampling plan measuring 23 steps is shown in figure 13(b). For both sample plans, five sites per field are measured to characterize intrafield modeling terms. Individual recipes with specific metrology structures, product layouts and sampling plans can be saved on the stepper.

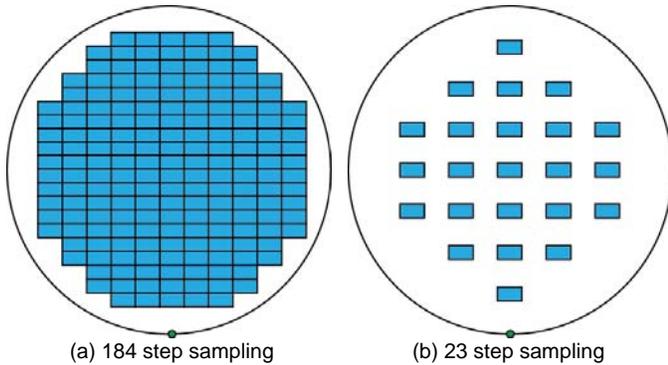


Figure 13: DSA-SSM sampling size (a) dense sample of 184 steps, 920 total points, (b) sample of 23 steps, 115 total points.

Overlay Optimization

The DSA-SSM measurements were used to optimize the TSV print in the TSV-last process. Direct referencing of the TSV print to the embedded METAL pattern allowed for identification of several critical parameters. System matching to a standard reference corrects for repeating linear and non-linear stage effects. For specific process optimization, linear corrections are available at the job level. For high doses thermal effects heat up the reticle and the lens which can affect overlay.

Optimization for the above mentioned effects are common for frontside overlay; and as DSA overlay approaches the performance of frontside overlay it is not surprising that detailed optimization is required for DSA alignment as well. For each of these activities the DSA-SSM metrology provides feedback to identify error components and estimate offsets to minimize their effects.

To simulate production operation, a lot of 10 wafers was run on the stepper, and the developed wafers were then analyzed using DSA-SSM with dense sampling. TIS measurement done on wafer 5 is -155nm and -453nm for X and Y respectively, and data from wafer 5 of this lot were used to construct figures 11 and 12. The TIS corrected vector map for one wafer (wafer 4) is shown in figure 14, and a summary table of overlay performance for the lot is shown in table 1. To examine the effect of sampling density the same data was sub-sampled to give a 23 step sampling which is summarized in table 2.

The average of the wafer 3σ is 765 and 559 nm for X and Y respectively, which can be reduced by adjusting linear grid

terms to give an estimated residual error of 756 and 368 nm for X and Y respectively. The larger residual error is in the X direction. If the X 3σ can be reduced to the level of the Y 3σ then the 750 nm overlay goal will be met.

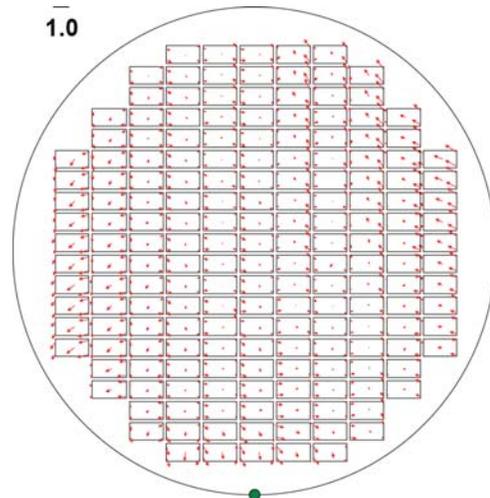


Figure 14: Overlay vector map for wafer 4 of 10. Data is after TIS correction of the mean. Wafer 4 is even numbered which has lower residual per wafer than the odd numbered wafers in the lot.

Wafer	X Avg	Y Avg	X 3σ	Y 3σ
1	0.241	0.005	0.867	0.654
2	0.027	0.018	0.662	0.627
3	-0.028	-0.079	0.845	0.657
4	-0.064	-0.056	0.658	0.515
5	-0.126	-0.040	0.859	0.543
6	-0.052	-0.010	0.680	0.561
7	-0.096	-0.053	0.871	0.536
8	-0.118	-0.053	0.683	0.498
9	-0.125	-0.032	0.864	0.555
10	-0.144	-0.004	0.659	0.444
Average	-0.048	-0.030	0.765	0.599

Table 1: Overlay performance for the lot of 10 wafers (in microns) with dense sampling of 184 steps per wafer. Data is after TIS correction of the mean.

Wafer	X Avg	Y Avg	X 3σ	Y 3σ
1	0.305	-0.041	0.844	0.518
2	0.089	-0.029	0.628	0.486
3	0.039	-0.121	0.797	0.471
4	-0.004	-0.099	0.626	0.365
5	-0.058	-0.084	0.793	0.324
6	0.013	-0.050	0.628	0.411
7	-0.024	-0.102	0.815	0.355
8	-0.054	-0.096	0.630	0.343
9	-0.053	-0.074	0.814	0.345
10	-0.082	-0.049	0.628	0.300
Average	0.017	-0.074	0.720	0.392

Table 2: Overlay performance for the lot of 10 wafers (in microns) with reduced sampling of 23 steps per wafer. Data is after TIS correction of the mean.

Comparing tables 1 and 2, the denser sampling plan shows a larger X and Y 3σ . The non-linear error signature, and having more sites near the wafer edge for the dense

sampling plan contributes to the difference between the two sampling plans.

An analysis of the X errors reveals non-linear errors that originate outside of the lithography module. Non-linear error can be characterized by looking at the residuals, which are the theoretical errors remaining after optimization of all possible linear grid terms and intra-field terms. Residuals can be random errors or non-correctable patterns. The per wafer residual analysis confirms a distinct alternating pattern shown in figure 15, with odd numbered wafers having much higher X residual. This pattern is also apparent in the per wafer residuals vector plot for wafers 4 and 5 as shown in figures 16 (a) and (b). Table 3 compares the per wafer residuals for the odd wafers and even wafers in the lot. The odd numbered wafers have a $3\sigma_x$ of 699nm and the even numbered wafer have a $3\sigma_x$ of 464nm. This pattern is dependent on the incoming wafer order, and changing the wafer sequence on the lithography system has no effect on the odd/even pattern. This is an example of an effect that cannot be easily identified without automated in-line metrology. Investigation into the root cause of the odd/even error source is ongoing.

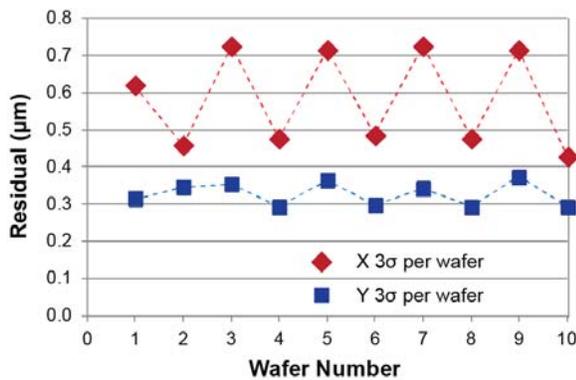


Figure 15: Per wafer residuals analysis (in microns) of a 10 wafer lot shows a strong odd/even wafer effect in X. To a lesser extent this odd/even effect can also be seen in the raw 3 sigma data.

Odd Wafers (1,3,5,7,9)		Even Wafers (2,4,6,8,10)	
Per wafer residuals 3σ		Per wafer residuals 3σ	
X	Y	X	Y
0.699	0.348	0.464	0.304

Table 3: Average of per wafer residuals (in microns) for ten wafers, separated by odd numbered and even numbered wafers.

Non-linear effects can be approached in various ways depending on the stability of the signature. For thinned substrates, significant distortions may come from processing steps other than lithography. Therefore the initial lithography matching may need to be supplemented with methods to address process specific higher order errors. Subdividing the wafer map into multiple alignment zones provides a flexible method to account for non-linear effects, because it allows for independent mapping and optimization of each zone [10]. The multi-zone approach can track errors that are not repeatable over time. The repeatable component of error can be addressed using non-linear offsets.

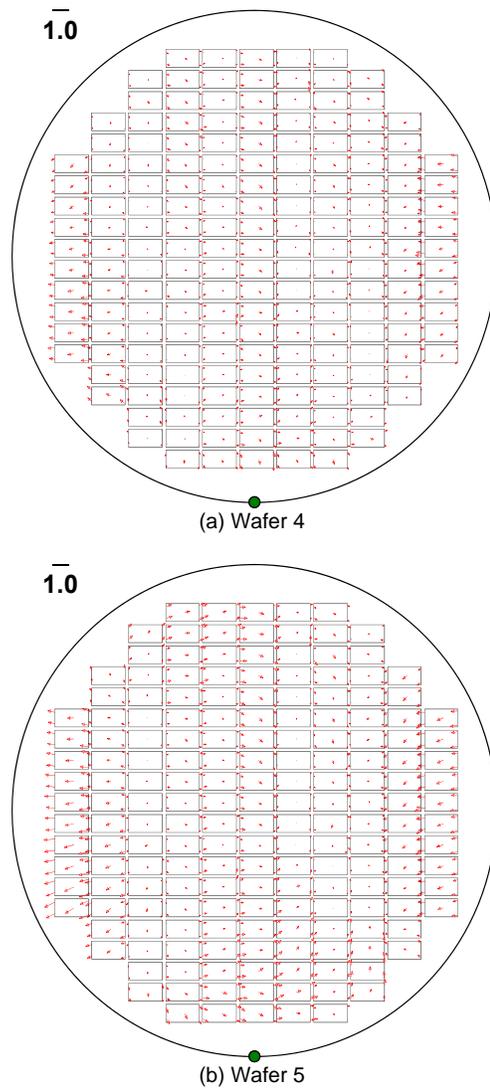


Figure 16: Per wafer residuals vector map for (a) wafer 4, and (b) wafer 5. Visually non-linear trends in the errors can be observed, and the odd numbered wafer has larger errors than the even numbered wafer.

To investigate the effectiveness of multiple alignment zones, the same wafer lot was processed through lithography again using a four quadrant mapping for each wafer as shown in figure 17. Each of the four quadrants can be independently mapped and optimized with linear stepper offsets. The improvements possible using four quadrant mapping is summarized in Table 4 and Table 5 for an odd numbered and even numbered wafer respectively. Of note, the difference in mapping method did not significantly improve the raw data overlay; however significant gains can be obtained by optimizing the per-wafer or per-quadrant offsets, and the use of per-quadrant offsets provides a better fit to non-linear errors.

Using overlay metrology and standard offsets provides a consistent method for overlay improvement, and the goal of 750nm overlay in production appears achievable by means of further error reduction. The data indicates that gains are possible in the areas of wafer order effects, non-linear wafer

signature, and transient thermal effects. Thermal effects can be minimized by going to a chemically amplified resist, which is currently being evaluated.

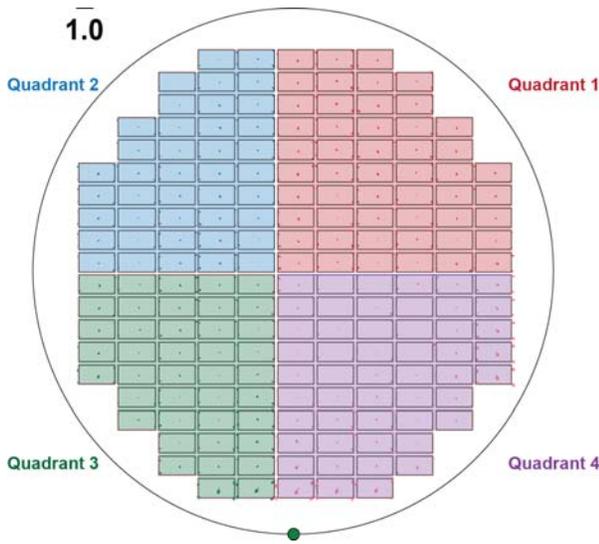


Figure 17: Per-quadrant residuals plot of wafer 5 processed on the stepper with four quadrant mapping.

Wafer 4 Run Type	Raw Data		Wafer Residual		Quadrant Residual	
	X 3 σ	Y 3 σ	X 3 σ	Y 3 σ	X 3 σ	Y 3 σ
Standard Alignment	0.658	0.515	0.475	0.293	0.230	0.278
Four zone mapping	0.664	0.557	0.332	0.358	0.187	0.264

Table 4: Comparison of standard alignment mapping and four quadrant mapping for an even numbered wafer, wafer 4. All data is in microns.

Wafer 5 Run Type	Raw Data		Wafer Residual		Quadrant Residual	
	X 3 σ	Y 3 σ	X 3 σ	Y 3 σ	X 3 σ	Y 3 σ
Standard Alignment	0.859	0.543	0.715	0.362	0.293	0.278
Four zone mapping	0.693	0.553	0.338	0.359	0.201	0.266

Table 5: Comparison of standard alignment mapping and four quadrant mapping for an odd numbered wafer, wafer 5. All data is in microns.

CONCLUSIONS

Scaling of TSV's in the TSV-last process requires tighter specs on overlay. With dimensions approaching the resolution limit of the stepper, the required overlay approaches the tool performance for frontside alignment. Direct verification of TSV lithography to the embedded reference layer is enabled by using the DSA alignment system combined with dedicated analysis software. This reveals that overlay correction methods commonly used for frontside lithography will become increasingly important for TSV lithography. Also, non-linear effects on alternating wafers can be a limiting factor in the achievable overlay performance. On good quality wafers the overlay performance is better than 750nm which is required for less than 5 μ m diameter TSV's.

ACKNOWLEDGMENTS

We would like to thank Stefaan Van Huylenbroeck for creating the test material and support on data analysis. We would also like to thank Patrick Jaenen for processing the chemically amplified resist material and Ellen Van Puymbroeck, Sara Moller and Kim Van Oostveldt for assisting in the measurements.

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