MICROBUMP LITHOGRAPHY FOR 3D STACKING APPLICATIONS

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ABSTRACT
3D packaging solutions are expected to play an important role in delivering improved performance, smaller form factors, and reduce costs for advanced semiconductor devices. The physical stacking of die-to-die or die-to-wafer requires high interconnect density. Aggressive scaling of microbump diameters and pitch is essential to meet these interconnect requirements. Maintaining process control for microbump lithography is challenging due to the small bump diameters and high aspect ratios. Since lithography is one of the important process sequences affecting final product yield, it is especially important to control the photoresist side wall profile and critical dimensions (CD). This paper will evaluate the use of stepper technology to meet the lithographic process control requirements for microbump applications.

Silicon wafers with Cu seed layer were used as a test vehicle to closely match the features of an advanced microbump product. The photoresist is a positive acting material coated to a thickness of 13 μm. Microbumps with a CD of 3.5 μm on a 10 μm pitch were exposed on the test wafers using a 1X stepper. CD metrology at the bottom and top of the photoresist was performed using a top down CD-SEM. The photoresist profile results were confirmed by cross sectional SEM analysis.

A process latitude evaluation was performed by varying the exposure dose and focus offset for each field across a wafer. The lithographic process window was obtained by analyzing the resulting focus versus exposure matrix. The optimal lithography conditions were determined from this process window. These conditions were then monitored using CD metrology in a fabrication environment. The stability of the process was demonstrated over an extended period using the top CD for statistical process control (SPC).

The experimental photoresist profiles through focus and exposure were also compared with optical lithographic simulations using Prolith modeling software by KLA-Tencore. The simulation results were validated by matching the experimental process window at the same process conditions. Photoresist simulation was then used to evaluate conditions beyond the experimental process such as smaller CD and pitch. The effect of photomask biasing to enhance process latitude was also investigated.

The experimental and modeled CD and side wall profile demonstrate a robust lithographic process for next generation microbump applications.

Key words: Microbump, 3D Packaging, Process window, Aspect ratio, Photoresist modeling, Statistical process control

INTRODUCTION
Over the last four decades Moore's law that the number of transistors in a device doubles every two years has largely been met by shrinking gate dimensions and decreasing operating voltage. However, below 28 nm design rules traditional front end device scaling is becoming increasingly complex with a significant impact on costs. As a result semiconductor manufacturing companies are focusing on various advanced packaging technologies which can help provide improved system level performance in a cost effective manner. One such technology is 3D chip stacking, where high density 3D interconnects are used between chip circuit blocks to create a die stack. This approach effectively enables high density scaling, reduces interconnect delays, improves bandwidth and power management [1,2]. An additional advantage of 3D chip stacking is that it enables the use of multiple technologies for various chip blocks to create a system level solution as shown in figure 1.

The implementation of 3D chip stacking in a manufacturing environment requires technology solutions for multiple issues including formation of Through Silicon Vias (TSV), wafer thinning, and fabrication of high interconnect density for the die-to-die stacking [2]. This study will investigate lithographic issues associated with forming the permanent electrical connections between the input and output pads of a die to the adjacent die above and die below it during the flipchip stacking process as shown in figure 2. Microbumps are required to meet the high interconnect density for 3D

stacking [2]. Microbumps are similar to copper pillar flipchip bumps. They are fabricated by electroplating a copper pillar on the under bump metallization (UBM) followed by a Tin based solder cap on top of the copper pillar [3,4].

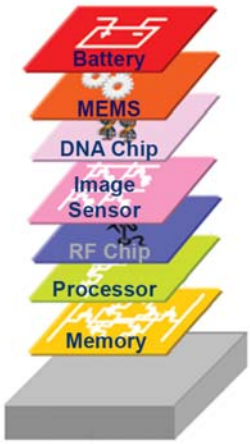

Figure 1: 3D stacking provides heterogeneous integration of different chip blocks to provide a complete a system on chip solution [2].

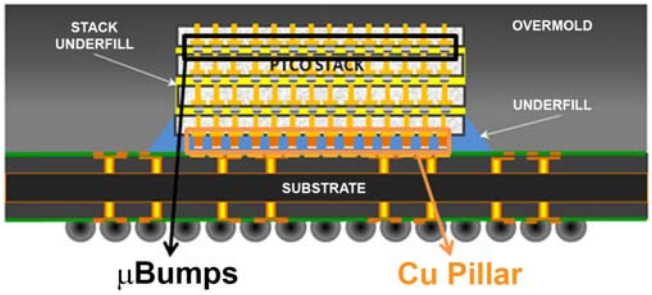

Figure 2: Drawings of a typical 3D stack showing the microbumps and Cu pillars.

Microbumps require the bump diameter and pitch to be dramatically reduced compared to standard copper pillar flipchip bumps. A summary of the process flow is shown in figure 3. The UBM or seed layer is deposited as shown in brown in 3(a). In 3(b) the photoresist shown in blue needs to be very thick compared to the critical dimension (CD) of the photoresist via hole for the microbump. A typical photoresist thickness to CD aspect ratio would be about 4 to 1 while maintaining the photoresist sidewall nearly vertical. The microbump shown in gold color is typically only electroplated to about 70% of the photoresist height as shown in 3(b). The CD at this height determines the top CD of the microbump. Finally the photoresist is stripped and the UBM etched as shown in 3(d). It is clear from this process flow that the critical lithography issues are the control of the CD and the photoresist sidewall angle for this thick photoresist.

In this paper, the state-of-the-art in microbump lithography will be reviewed and an outlook into the further development roadmap for 3D stacking will be presented.

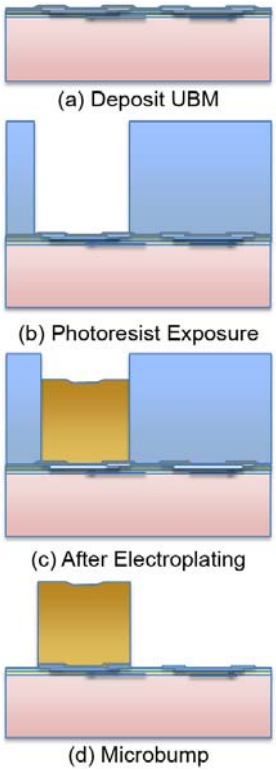

Figure 3: Process Flow showing (a) the deposited UBM (brown), (b) photoresist (blue) after development, (c) after Cu and solder electroplating (gold) and (d) the final bump after photoresist strip and UBM etching.

EXPERIMENTAL METHODS

Equipment

Lithography was performed on an Ultratech AP300 advanced packaging stepper with a 0.16 numerical aperture (NA) Wynne Dyson lens. This unique design permits the use of broadband illumination from a mercury arc lamp, and the system used in this study has a capability to select different wavelengths: i-line, gh-line or ghi-line [5]. The tool is also equipped with a WEE (Wafer Edge Exposure) unit for exposing the edge of the wafer and a WEP (Wafer Edge Protection) unit for protecting a predefined outer edge of the wafer. The WEE enables precise removal of photoresist on the edge of the wafer where electrical contact is required during electroplating. The WEP blocks exposure and is used to retain photoresist on the inside the WEE ring creating a protective seal or dam ring to prevent leakage of plating solution during the electroplating step.

All photoresist processing is performed on a TEL ACT12 Clean Track which is equipped with high viscosity pumps for thick photoresist coating.

Reticle

For this study a reticle was selected that is currently used as part of a test chip for 3D packaging. The reticle was designed for microbump creation by electroplating Cu inside via holes printed in the positive tone photoresist. Size variation of vias will influence the characteristics of the

electroplating process. To produce the best uniformity, a common via design is used throughout the device. The design on the reticle consists only of round via holes with a fixed pitch of 10µm, and a diameter of 3.5µm.

Processing

Test wafers for this study were prepared with a typical seed layer of 150nm Cu. The photoresist selected was positive tone AZ EM 10XT coated to a thickness of 13.2µm as measured after softbake. A FEM (Focus Exposure Matrix) was created on the test wafers to evaluate the affect of lithography exposure dose and focus on the resulting photoresist pattern. In the FEM wafer layout, the focus offset (µm) is varied along the X axis while the exposure dose (mJ/cm^2) is varied along the Y axis as shown in figure 4. This allows a wide range of lithography conditions to be evaluated on a single wafer. The photoresist does not require a PEB (post exposure bake) and is developed using AZ400K (KOH based) diluted 1 to 4 with water.

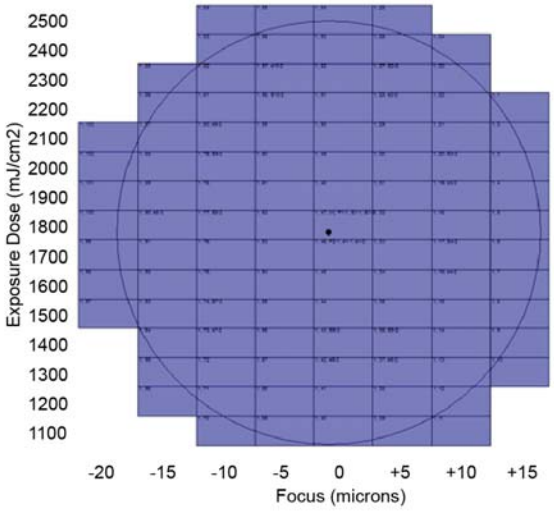

Figure 4: Wafer layout for the FEM. An eight by fifteen array was exposed with focus varying in the horizontal axis and exposure dose varying in the vertical axis.

Each array location on the completed FEM wafers were then measured using a top down scanning electron microscope (SEM) to determine the CD at 0% and 100% of the photoresist thickness. In addition, cross sectional SEM metrology was performed at 0%, 10%, 90% and 100% of the photoresist

Analysis

The SEM data from the FEM wafers was analyzed using ProDATA CD software by KLA-Tencor. A Bossung curve analysis can be constructed by plotting the measured CD against the focus offset (microns), with data points having the same exposure energy (mJ/cm^2) plotted on one curve [6]. This format allows quick visual appreciation of the data and enables further processing with curve fitting and process window analysis.

The process window is defined as the variation around a chosen setting that gives performance within a predefined range. Typically in lithography the maximum allowed CD variation is set at ±10% of the nominal CD, and a minimum photoresist sidewall angle is specified to support the etch or electroplating process. These two criteria are typically specified for determining depth of focus (DOF) of the process.

RESULTS AND DISCUSSION

The Focus/Exposure Matrix

Bossung plots were generated using bottom CD data collected from the top down CD SEM in Figure 5 and collected from the cross sectional SEM in figure 6. They both show the response of the photoresist process through focus offset and exposure dose using the bottom CD criteria of 3.5 ± 10% µm (red horizontal lines). The nominal conditions appear to be around 1800 mJ/cm^2 (purple curve with triangle data markers) and zero focus offset from the top down CD SEM.

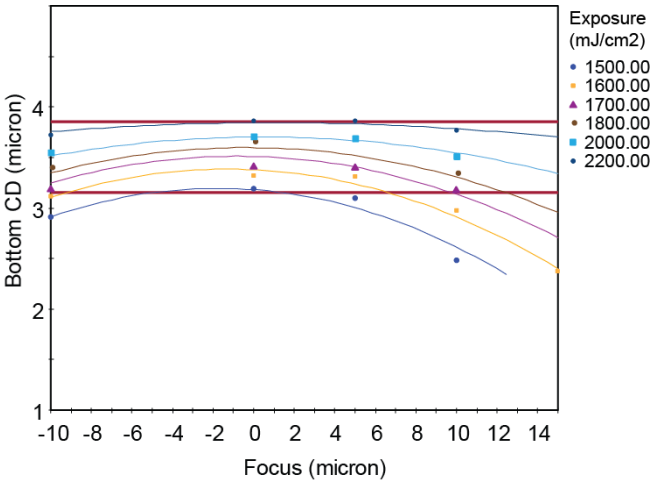

Figure 5: Bossung Plot for 3.5 µm via hole with a pitch of 10µm using bottom CD data from top down CD SEM.

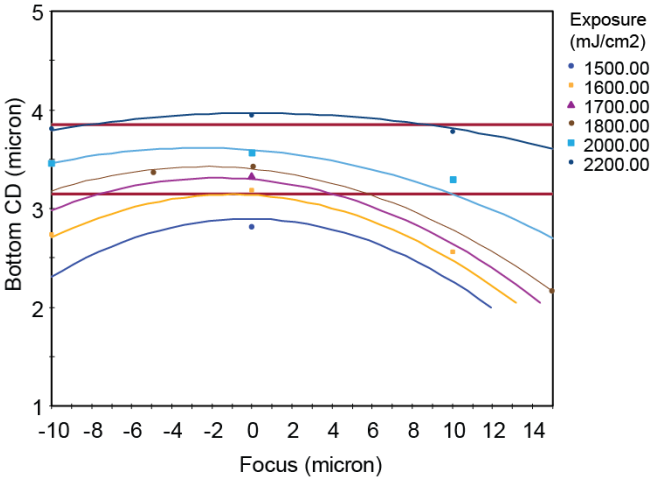

Figure 6: Bossung Plot for 3.5 µm via hole with a pitch of 10µm using bottom CD data from cross sectional CD SEM.

The results from the cross sectional SEM (figure 6) show a wider spread of CD as compared to top down SEM (figure 5) through both exposure and focus. This is most likely due to the difficulty of data collection for cross sectional via hole analysis. If the round resist openings are not cleaved through the via center the cross sectional measurement data are less accurate. The cross sectional SEM measurements also give significantly smaller CD results than top down SEM at lower exposure doses but are more closely matched at higher exposure doses. This resulted in a 195 mJ/cm^2 difference in nominal dose for the 3.5 µm target CD as calculated by ProDATA for the two metrology methods. Another cause for the difference in CD readings is the slight photoresist footing that is observed when the via hole openings are cleaved but is not detected using the top down CD SEM.

Process Windows

It is clear from the process flow in figure 3 that the critical lithography issues are the control of the CD and the photoresist sidewall angle. The bottom CDs and sidewall angles calculated from cross sectional CD can be used to construct a process window as shown in figure 7. The CD target is 3.5 µm ± 10% (yellow dashed envelope) and the sidewall angle specification is ≥ 87 degree (purple dashed envelope). In this case, the overlap process window where both constraints are met (blue envelope) indicates that the sidewall angle of 87 degree is the limiting factor in determining the DOF. The red box is the largest rectangular process window centered at the nominal CD of 3.5 µm (blue dashed curve) that fits within the overlap envelope region. The width of the red box corresponds to the DOF, which in this case is 10.0 µm.

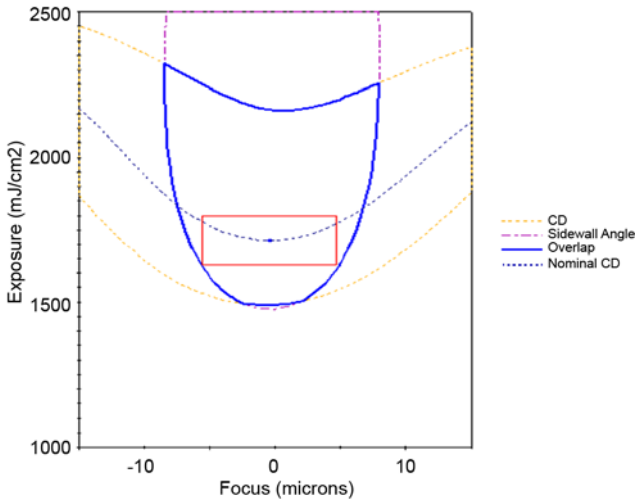

Figure 7: Experimental process window for 3.5 µm via using bottom CD data with a pitch of 10 µm and a photoresist thickness of 13.2 µm. The DOF is 10.0 µm with a nominal exposure dose of 1700 mJ/cm^2. Sidewall angles were determined by cross sectional CD SEM.

Detailed characterization of thick photoresist processing is best done using the cross sectional SEM analysis. However, monitoring the photoresist process using cross sectional CD is time consuming and is not practical in a manufacturing environment. While the cross sectional CD measurements showed stronger response to focus change, results in both figures 5 and 6 give the same best focus offset close to zero. Thus by keeping the stepper focus control to ± 3 µm, the process can be monitored by top down CD SEM.

Lithography Simulation Matching

Using Prolith lithography simulation software by KLA-Tencor, a positive photoresist model was generated to match the experimental cross section SEM data. Figure 8 shows a simulated process window for 3.5 µm round vias at a pitch of 10 µm, in 13.2 µm thick photoresist.

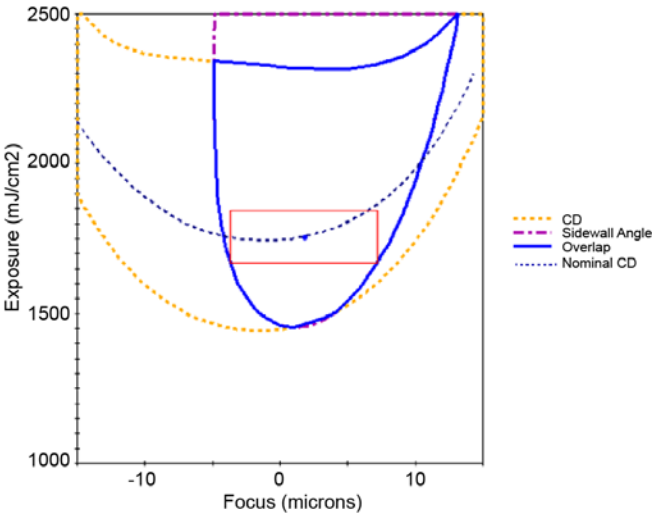

Figure 8: Modeled process window for 3.5 µm via at 10 µm pitch and resist thickness of 13.2 µm. The DOF is 10.86 µm with a nominal exposure dose of 1750 mJ/cm^2.

The CD target is 3.5 µm ± 10% measured at the photoresist base (yellow dashed envelope), and 87 degree sidewall angle (purple dashed envelope). The simulation shows a large overlap region (blue envelope) where CD and sidewall angle specifications are simultaneously met. Again, the red rectangular box denotes the DOF centered at the nominal CD (blue dashed curve). For this case the DOF is 10.86 µm which is slightly larger than the experimental results of 10.0 µm determined in figure 7. The nominal exposure dose is 50 mJ/cm^2 larger than the experimental dose determined in figure 7.

Figure 9 shows experimental and simulated cross sections of 3.5 µm via holes on a 10 µm pitch through a 30 µm range of focus offsets. At -15 µm focus the via exhibits a large flair at the top of the photoresist which reduces the sidewall angle. At +15 µm focus the via exhibits more footing at the bottom of the photoresist which also reduces sidewall angle. The via hole shape through focus exhibits good correlation between the experimental and simulated results.

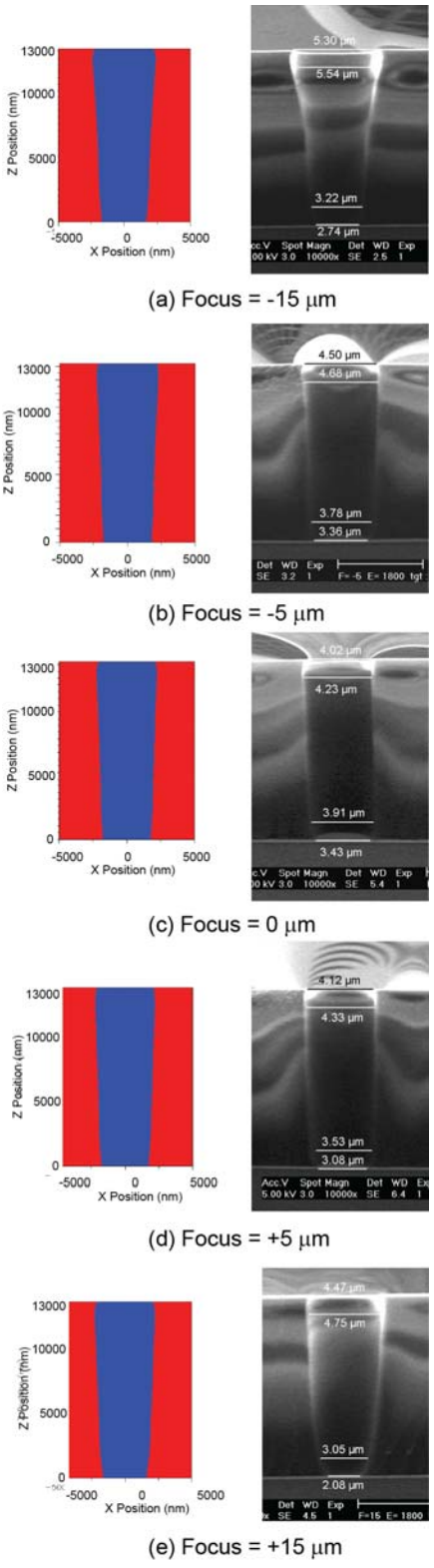

Figure 9: Comparison of simulated and experimental photoresist cross sections of 3.5 µm vias through -15 to +15 µm focus offsets. The photoresist thickness is 13.2 µm and the exposure dose is 1800 mJ/cm^2.

Extending Lithography Simulations

A well calibrated lithographic model allows evaluation of conditions beyond the current experimental process. Additional simulations were generated to determine how AZ EM 10XT photoresist would perform at smaller via hole diameters and pitch. The process windows for 3.0 and 2.5 µm round vias is shown in figures 10 and 11 respectively. For these simulations the photoresist thickness and feature pitch are scaled in proportion to the CD.

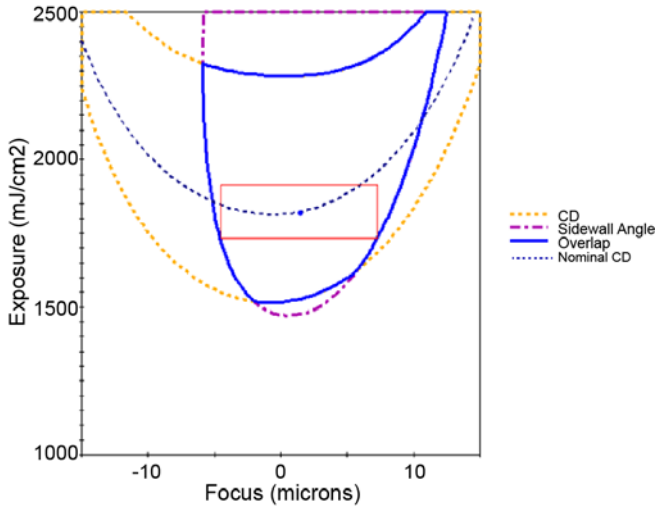

Figure 10: Modeled process window for 3.0 µm via at 8 µm pitch and photoresist thickness of 11.3 µm. The DOF is 11.77 µm and the nominal dose is 1825 mJ/cm^2.

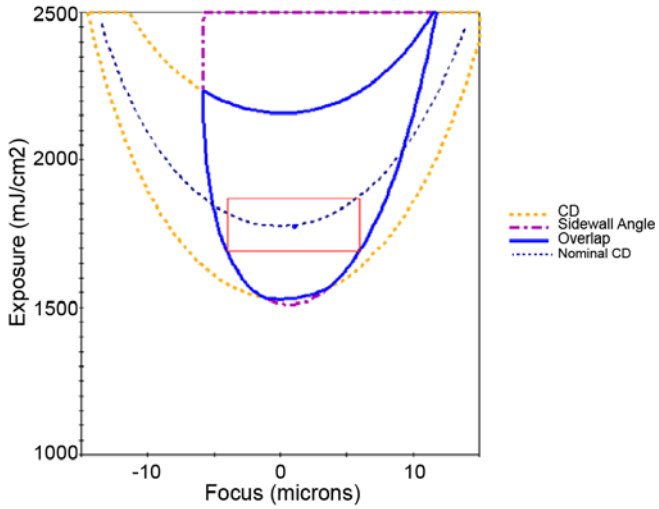

Figure 11: Modeled process window for 2.5 µm via at 6 µm pitch and photo resist thickness of 9.4 µm. The DOF is 9.93 µm and the nominal dose is 1775 mJ/cm^2.

At 3.0µm CD the DOF is 11.77 µm which is larger than the 10.86 µm observed for the 3.5µm CD in figure 8. This is due to the difference in photoresist thickness. At 2.5 µm CD the DOF has decreased to 9.4 µm. However, this is still sufficient DOF for a robust lithography process.

The effect of photomask biasing can also be investigated. A reduction of the mask feature size by 0.1 µm smaller than the 2.5 µm via hole size increased DOF to 12.32 µm as shown in figure 12. However, the nominal exposure dose increases from 1775 to 1975 mJ/cm^2 which could reduce the overall throughput of the lithography cell.

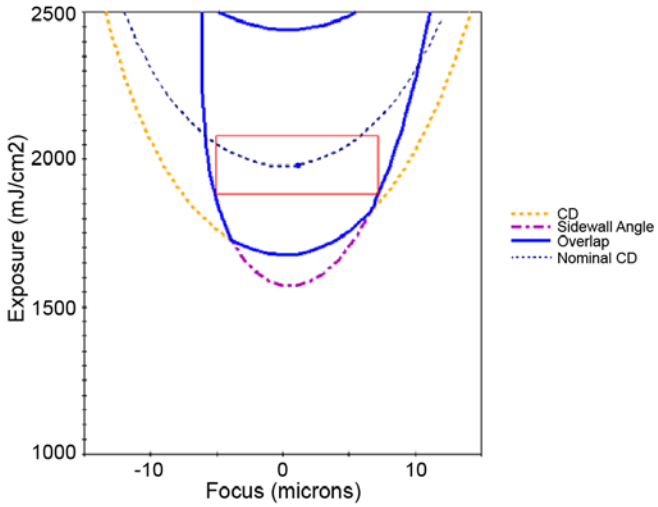

Figure 12: Modeled process window for 2.5 µm via at 6 µm pitch using a biased 2.4 µm feature on reticle. This increases the DOF from 9.93 to 12.32 µm. This nominal dose increases to 1975 mJ/cm^2.

Process Control

Daily monitoring of the photoresist process can be performed using top down CD SEM metrology. For electroplating purposes the CD near the base of the via hole is more important for process control than the top CD. However, for the high aspect ratio vias used in microbumps the top CD is often easier to measure than the bottom CD as shown in figure 13. As a result for a well characterized process the top CD can serve as an effective measurement for process control.

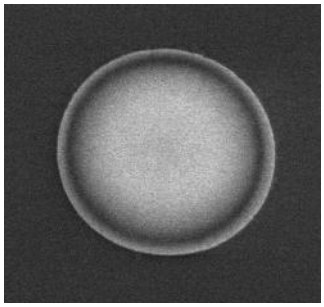

Figure 13: Top down SEM image of a 3.5 µm via at nominal conditions of 1800 mJ/cm^2 and zero focus.

The effect of focus and exposure dose on top down CD SEM measurements is shown in figure 14. The contours show the top CD in microns and the dashed box is the process window defined in Figure 7 using bottom CD data. It is clear that there is a large window of process stability using top CD SEM measurements. The effect of focus offset on CD at 1800 mJ/cm2 dose is shown in figure 15. The bottom CD has a local maximum at zero focus offset and the top CD has a local minimum at 5 µm focus offset. These characteristic curves can be used to interpret variations in CD measurements. Note that focus calibration is independently maintained as part of routine stepper maintenance.

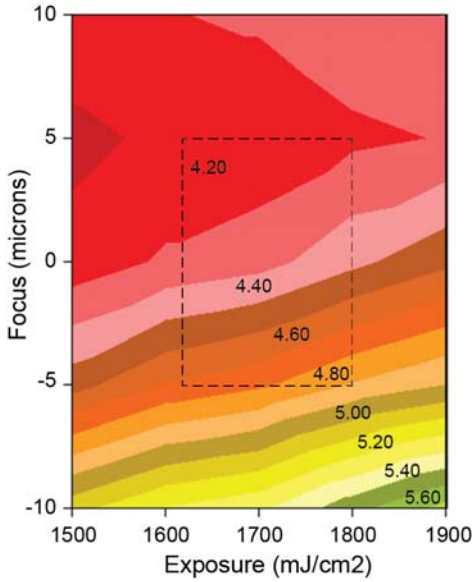

Figure 14: Contour plot of top CD data (µm) as a function of Focus and exposure for 3.5 µm via with a pitch of 10 µm and a photoresist thickness of 13.2 µm.

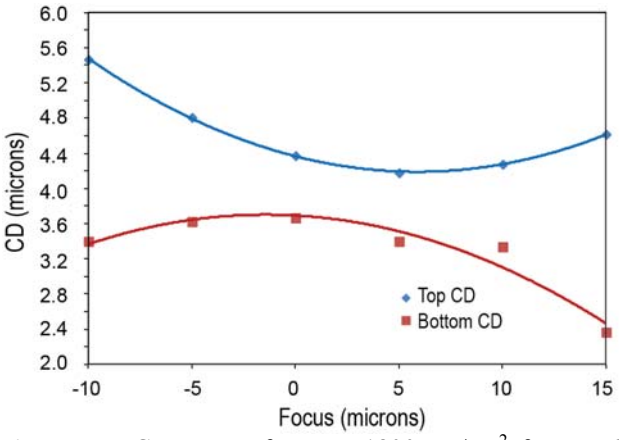

Figure 15: CD versus focus at 1800 mJ/cm^2 for top CD (blue) and bottom CD (red) for 3.5 µm via with a pitch of 10 µm and a photoresist thickness of 13.2 µm as measured with top down CD SEM.

Statistical Process Control Charts

Statistical process control (SPC) was performed on Cu-seed test wafers. Both top CD and bottom CD were measured in fully automatic mode on a KLA 8250 CD-SEM, whereas the FEM data measurements used a manual mode.

For each wafer top CD and bottom CD are measured on nine locations and the average and range are plotted on

control charts. The Average Control Chart in figure 16 describes the stability of the wafer to wafer performance. The Range Control Chart in figure 17 describes the stability of the within wafer performance. The average and range data are summarized in Table 1.

	Top CD	Bottom CD
Mean of Averages	4.34 µm	3.48 µm
Standard Deviation Averages	21 nm	67 nm
Moving Range of Averages	25 nm	45 nm
Average Within Wafer Range	36 nm	446 nm
# samples / wafer	9	

Table 1: Within wafer average and range for Top CD and Bottom CD measurements.

The measured within wafer CD range is much larger for the bottom CD than for the top CD. The bottom CD measurements show much more variation than the top CD measurements, and this discrepancy is attributed to measurement error for the bottom CD measurement. One issue that makes measuring the bottom CD more difficult in automatic mode is that the SEM performs auto focus on the top surface of the resist, which then requires a focus offset to achieve good focus for the bottom measurement. Also, contrast at the bottom of a deep opening is less than at the top, and the resist footing makes the bottom edge of the resist less distinct as can be seen in figure 13. The result is a larger uncertainty in bottom CD due to measurement error. Since the top CD measurements have less measurement error, the control charts were constructed using top CD measurements.

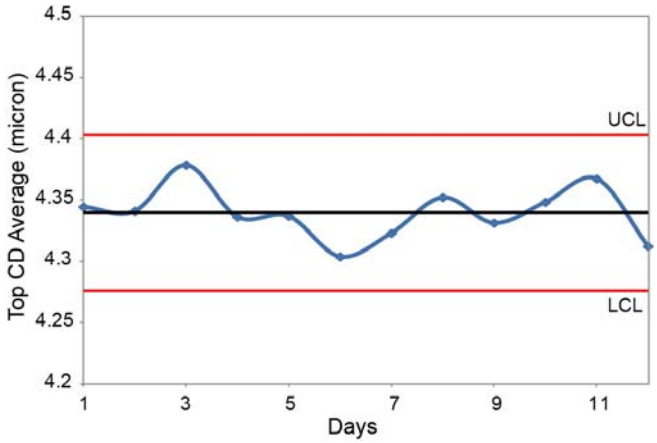

Figure 16: Average control chart for top CD showing the stability of the wafer to wafer performance.

The Top CD measurements indicate that the process has good within wafer uniformity and stability. Figures 16 and 17 indicate that the process is in statistical control. Process limits are typically set at ± 10% CD for the bottom CD and corresponding process limits for the Top CD are extracted from the process window data summarized in figure 14. Process limits for top CD may vary from 4.2 to 4.8 µm. The control limits have a much tighter range than the process range.

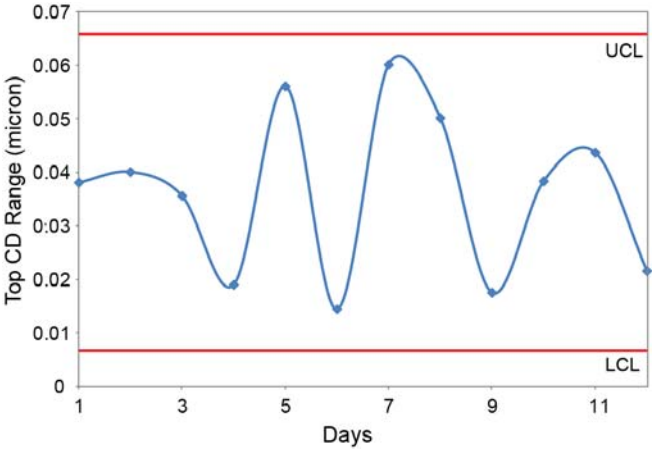

Figure 17: Range control chart for top CD showing stability of within wafer performance.

CONCLUSIONS

Silicon wafers with copper seed layer were used as a test vehicle for evaluating lithography performance for an advanced 3D stacking application. The target application requires 3.5 µm wide copper plugs on a 10 µm pitch, with a 5 to 9 µm height. The process creates high aspect ratio holes in thick photoresist, and these holes are partially filled to form copper plugs. To maintain the desired plug dimensions, the diameter and sidewall angle of the photoresist opening must be tightly controlled. Top down and cross section SEM photos were taken across a range of stepper focus and exposure conditions to determine the practical lithography process window. At the target CD value of 3.5 µm and a minimum sidewall angle of 87 degree, the photoresist process provides a large depth of focus. The cross section measurements exhibited more variation than top down methods, and this may indicate difficulty in cleaving through the center of the round vias. From top down SEM, the bottom CD measurements provide good correlation to lithography modeling. The model was used to simulate process windows for smaller vias, and to investigate the potential benefits of biasing the mask. For in-line process monitoring the top CD provided more consistent measurements than the bottom CD, and therefore the top CD was used to generate process monitor control charts. Process monitor data shows ability to maintain consistent CD control over time.

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