External Resistance Reduction by Nanosecond Laser Anneal in Si/SiGe CMOS Technology

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***Abstract*—**We report on a significant pFET external resistance reduction (~40%) and corresponding 10% R_{ON} decrease by nanosecond laser annealing of S/D structures applicable to advanced technology nodes. Selective melting of pFET S/D elements is responsible for this improvement. Process window boundaries are defined by channel and junction melting at the upper end and by S/D SiGe melting at the lower end. Short channel characteristics are not degraded within the identified process window. Contacted gate pitch (CPP) and fin number dependence of the process window is assessed.

I. Introduction

MOSFET parasitic resistance degrades rapidly as transistor dimensions approach the scaling limit. Shrinking volume of conductive elements, reduced interfacial area between these elements, and increased effective channel width (W_{eff}) in 3D transistor architectures lead to a significant increase in the external resistance (R_{EXT}). Fig. 1 illustrates components of FinFET external parasitic resistances in cross gate and cross fin directions. The R_{EXT} can be partitioned into S/D epi resistance (R_{EPI}), contact resistance (R_C), and MOL metal stud resistance (R_{METAL}). Much attention has been recently given to R_C and R_{METAL} exploring various approaches such as dual silicide for R_C reduction [1, 2] and cobalt contact stud for R_{METAL} reduction [2, 3]. While these are vital, R_{EPI} and R_C reduction is equally critical.

Laser annealing at the contact level has also been explored for R_C improvement [4-10] via forming interfacial dopant-semiconductor supersaturated metastable alloys through solid or liquid phase epitaxial (SPE/LPE) re-growth. Such laser-induced SPE/LPE processes yielded a record low contact resistivity at or below $1\times10^{-9}\,\Omega\cdot cm^2$ for both n-type and p-type contacts. Nanosecond-scale (nSec) laser melt annealing is particular promising technique for achieving such low resistivity in metal-semiconductor contacts but its implementation is hindered by a small process window and various layout dependences [10]. Hierarchy of materials melting points and other catastrophic failures define the process window. Low melting point materials such as SiGe may allow for an improved process window [11] and exploring nSec laser melt annealing for pFETs with high/mid percent Ge in SiGe S/D structures is strategically important in the context of practical implementation for advanced CMOS technologies.

In this work, we systematically examine the effect of nSec laser melt annealing on external parasitic resistance in advanced pFinFETs, determine the hierarchy of melting thresholds and their effect onto R_{EXT} improvement and CMOS process window, and reveal key process window dependencies on CPP and number of fins. pFET R_{EXT} is significantly reduced (~40%) by selective S/D melting at the contact level positively affecting both R_{EPI} and R_C.

II. 1D Epitaxial Films and TLM Structures

Blanket one dimensional epitaxial films were used to elucidate basic electrical response of nSec laser melt annealing and dopant activation and redistribution in the molten phase. 40-80nm of mid/high percent Ge SiGe epitaxial films were grown on n-Si substrate and implanted with a p-type dopant. Top ~7-10nm were amorphized by the implantation process. The implanted film was laser annealed at different incident energy densities (ED) corresponding to different surface peak temperatures. The sheet resistance response of the annealed film is shown in Fig. 2. Three distinct regions correspond to re-crystallization of amorphous SiGe with a drop in R_S, no change in R_S upon raising surface temperature above amorphous SiGe re-crystallization threshold, further reduction in R_S upon melting crystalline SiGe underlayer with subsequent dopant redistribution and activation. This response is typical for this material system with a thin amorphized layer and qualitatively does not change with Ge content in SiGe and the type of p-type dopant as long as the dopant has a high solubility limit in SiGe and is present in abundance well above its solubility limit. In addition to R_S, the semiconductor-metal contact resistivity ρ_C has also been assessed for this basic material system using TLM structures. The SiGe epitaxial film is covered with a silicon oxide isolation (ILD) layer and contact trenches are etched in the ILD layer at different distances to each other forming the basis for the TLM measurement. The base epitaxial film is implanted through the contact trenches creating doped amorphous pockets as schematically shown in Fig. 3. The implanted film was laser annealed at different energy densities corresponding to different SiGe film temperatures. Fig. 4 shows evolution of amorphous pocket as it is subjected to progressively higher laser energy density. Fig. 4a shows initial amorphous pocket after implantation. Fig. 4b shows a partial re-growth at a low laser energy density. Fig. 4c shows a full re-growth at an intermediate laser energy density. Fig. 6 is a dark field STEM image of a formed contact corresponding to the laser energy density employed in Fig. 4c. Re-distribution of Ge can be seen in the re-crystallized pocket. Fig. 7 provides an elemental line scan of Ge distribution in re-crystallized a-SiGe pocket. Observed Ge segregation at the surface is an earmark of a-SiGe melting and LPE and is beneficial for reducing contact resistance. A further increase in the laser energy density leads to c-SiGe film melt. Fig. 5 shows the extracted contact resistivity including the resistance of contact metal stud. At a low energy density corresponding to partial re-growth, the ρ_C is high. At an intermediate energy corresponding to full re-growth and Ge segregation, the ρ_C is low. At a high energy corresponding to c-SiGe melting, the ρ_C increases again due to the contact dopant reduction in dopant redistribution process.

III. Fin Laser Melt Threshold

FinFETs structures have drastically different laser energy density melting thresholds than those of blanket films and basic TLM structures. This is due to their different optical reflectance and thermal conductance. Accordingly, the melting thresholds need to be re-established. In our case, pFETs have 4 basic materials with progressively higher melting points as shown in Fig. 8. Amorphous SiGe contact pocket (A) has the lowest melting point followed by that of crystalline SiGe source/drain (B), then by that of channel SiGe (C), and the highest melting point occurs in Si subfin region (D). Gross melting of regions (C) and (D) has been found by STEM imaging after laser exposure. Fig. 9 shows bright and dark field STEM images for determining laser energy density for such gross melting. Figs. 9-1a/1b show an incoming fin structure with SiGe active fin and Si subfin region. Figs. 9-2a/2b show an onset of channel SiGe melting showing channel defects in the bright field view and Ge striations in the dark field view. Figs. 9-3a/3b show a complete channel melt with numerous channel defects and an onset of Si subfin melt with a Ge re-distribution from the channel into the subfin. Figs. 9-4a/4b show a complete melt of Si subfin with Ge re-distribution deep into the subfin region and numerous defects in it. The laser energy density and substrate pre-heat temperature corresponding to Figs. 9-2a/2b were taken as an upper limit for electrical hardware.

IV. pFinFET Electrical Response

After contact implantation, pFETs were exposed to different nSec laser energy density with the interval corresponding to ~50-60°C step in annealing temperature up to the channel melt condition at the higher end. Figs. 10 and 11 show pFET R_{ON} and R_{EXT} response, respectively. The reference cell is the SPE pocket re-growth induced by a millisecond-scale laser annealing. There are two distinct regions corresponding to a smaller improvement at low nSec laser energy densities and a large improvement at higher energy densities. The cell corresponding to the highest energy density is not shown due to an electrical short.

Figs. 12 and 13 show corresponding changes in short channel characteristics: ΔDIBL and ΔSsat, respectively. Only the high energy cell exhibits a change in these parameters suggesting that the dopants started to penetrate into the channel at this energy density. Fig. 14 shows corresponding pFET I_{DSAT}-V_G curves. The highest energy density cell results in the source-to-drain electrical short suggesting that the S/D dopants penetrated deep into the channel and shorted it. The cell with the degraded DIBL and Ssat slope is clearly seen in this chart and points at the onset of dopant penetration into the channel. The remaining cells show varying degree of improvements.

Fig. 15 shows I_{DSAT}-V_G curves for nFETs with Si channel and source/drain. No changes in nFETs behavior is seen even at the highest energy density consistent with the absence of Si fin melting. Absence of Si fin melting is due to the energy density limit set in section IV and the difference between melting points of SiGe and Si.

V. Melting Threshold Hierarchy

Fig. 16 pictorially summarizes the observed melting hierarchy and its impact in pFinFETs. Fig. 16-1 is the incoming pFETs structure. Fig. 16-2 shows melt and re-crystallization of amorphized pockets with re-distribution of dopants and Ge in the pockets. It is this process that is believed to correspond to a smaller improvement of R_{ON} and R_{EXT} at low nSec laser energy densities. Fig. 16-3 shows melt and re-crystallization of crystalline SiGe source/drain structures with dopant re-distribution and activation. It is this process that is believed to correspond to a large improvement of R_{ON} and R_{EXT} at intermediate energy densities. Fig. 16-4 shows melt and re-crystallization of junctions adjacent to the SiGe channel with the dopants moving into the channel near gate edges. The SiGe junction may have a higher Ge content than that of the channel but less than that of source/drain. It is this process that is believed to correspond to degrading short channel characteristics. Fig. 16-5 shows melt and re-crystallization of the SiGe channel with the dopants moving deep into the channel. It is this process that is believed to correspond to shorting pFET channel. Fig. 16-6 shows melt and re-crystallization of the Si subfin and channel with the dopants and channel Ge moving into the subfin region.

VI. Layout Dependencies

The onset of degrading short channel characteristics defines the upper end of laser energy density. Accordingly, ΔDIBL can be used to assess a catastrophic layout effect that may induce a severe degradation of short channel effect in some common layouts. Figs. 17 and 18 show dependencies of ΔDIBL on fin number and CPP, respectively. No CPP dependence has been observed within the studied range. Transistor with reduced number of fins are more susceptible to the onset of DIBL degrade suggesting that they are heated to a higher peak temperature, as shown in Fig. 17. This is likely caused by a low thermal conductance in a FinFET with reduced number of fins. Reducing laser energy density by one interval eliminates this DIBL degradation pointing to less than ~50°C difference in annealing temperature between these transistors.

VII. Conclusion

In this work, we systematically examine the effect of nSec laser melt annealing on external parasitic resistance and short channel characteristics in advanced pFinFETs. R_{EXT} is significantly reduced (~40%) by selective S/D melting at the contact level positively affecting both R_{EPI} and R_C. Process window boundaries are defined by channel and junction melting at the upper end and by S/D SiGe melting at the lower end. Short channel characteristics are not degraded within this process window. Contacted gate pitch (CPP) does not affect the process window within the studied range and the fin number may induce a shift in the process window by roughly ~50°C.

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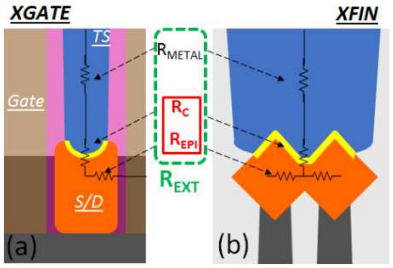

Fig. 1. External parasitic resistance (R_{EXT}) in FinFETs: (a) cross gate direction (b) cross fin direction. Focus of this work is on the epi (R_{EPI}) and contact (R_C) resistances.

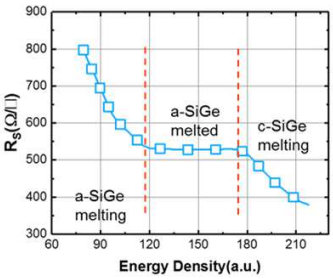

Fig. 2. Sheet resistance of implanted and laser annealed SiGe epi layers. Increasing laser power density results in 3 distinct regions. Laser exposure duration is ~60 nsec.

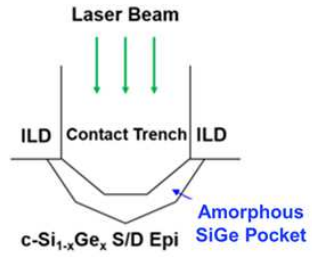

Fig. 3. Schematic of TLM structure for contact resistance measurement. Implanted amorphous SiGe pocket is re-grown via laser-induced LPE.

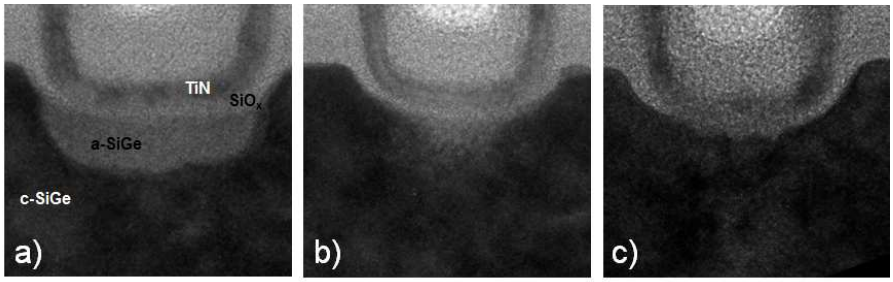

Fig. 4. TLM contact structures: a) after trench pocket amorphization; b) after laser exposure at an energy density (ED) of 67 - partially regrown; c) after ED = 86.1 exposure - fully regrown. ED refers to the incident energy density expressed in a.u. Laser exposure duration is ~60nsec. Substrate preheat did not result in a-SiGe recrystallization. TiN was used for STEM highlight without oxide removal.

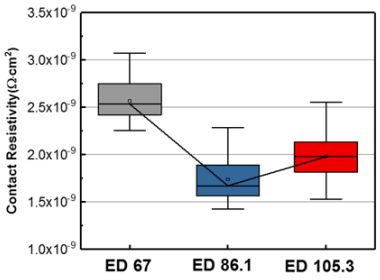

Fig. 5. TLM contact resistance as the function of incident energy density at laser exposure duration of ~60nsec. Metal stud resistance is not subtracted.

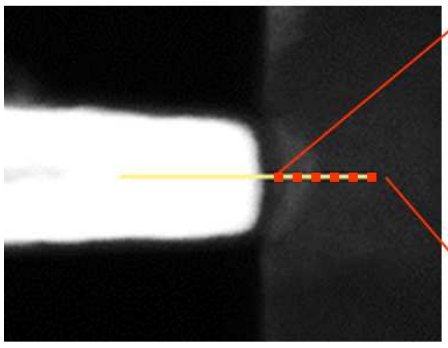

Fig. 6. Dark field STEM image of a formed contact using laser induced LPE at ED = 86.1.

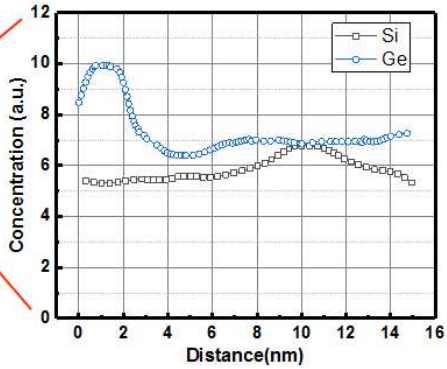

Fig. 7. Elemental line scan across the re-crystallized a-SiGe pocket. Ge segregates near the surface.

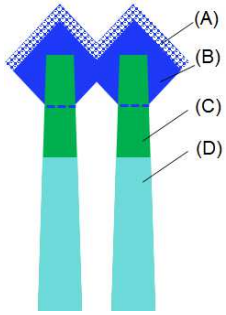

Fig. 8. Schematic of pFinFET highlighting materials with different melting points: (A) amorphous SiGe pocket; (B) SiGe S/D epi; (C) SiGe active fin; (D) Si subfin.

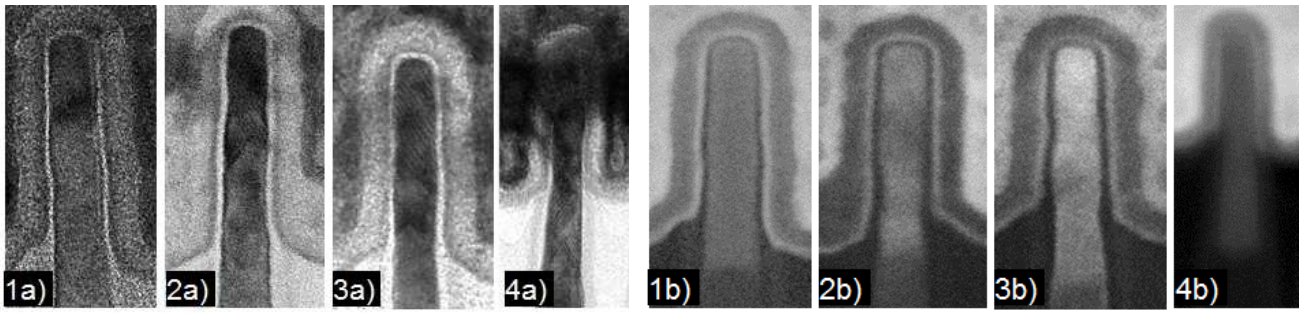

Fig. 9. Bright field ("a"-series) and dark field ("b"-series) STEM images of pFET fins: (1) prior to laser annealing; (2) after laser exposure at ED = 82.3 – signs of SiGe channel melting; (3) after exposure at ED = 105.3 – complete channel melting and signs of Si subfin melting; and (4) after exposure at ED = 95.7 and 100°C higher substrate base temperature – complete melting of fin and subfin regions and Si/SiGe mixing.

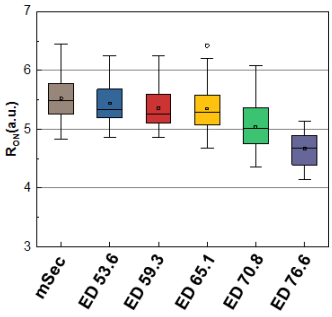

Fig. 10. pFET R_{ON} versus incident nSec laser energy density. Millisecond-scale (mSec) annealing serves as the reference.

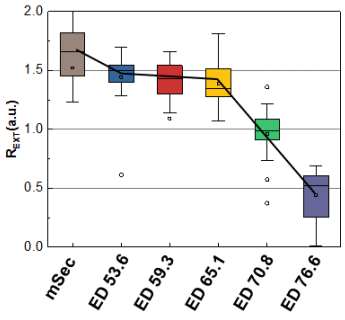

Fig. 11. pFET R_{EXT} versus incident nSec laser energy density. Millisecond-scale (mSec) annealing serves as the reference.

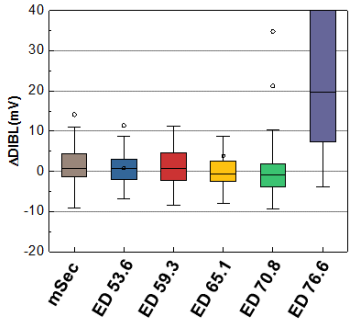

Fig. 12. pFET ΔDIBL versus incident nSec laser energy density. Millisecond-scale (mSec) annealing serves as the reference.

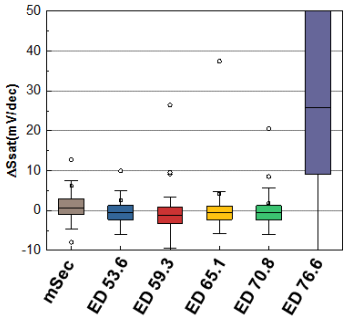

Fig. 13 pFET change in subthreshold slope (ΔSsat) versus incident nSec laser energy density. Millisecond-scale (mSec) annealing serves as the reference.

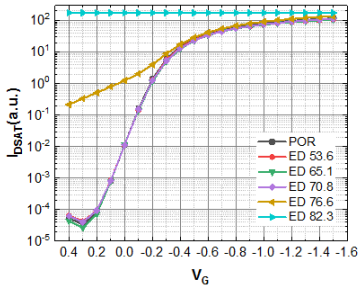

Fig. 14 pFET I_{DSAT}-V_G as the function of incident nSec laser energy density. Millisecond-scale (mSec) annealing serves as the "POR" cell.

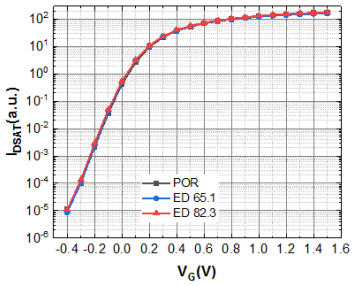

Fig. 15 nFET I_{DSAT}-V_G as the function of incident nSec laser energy density. Millisecond-scale (mSec) annealing serves as the "POR" cell.

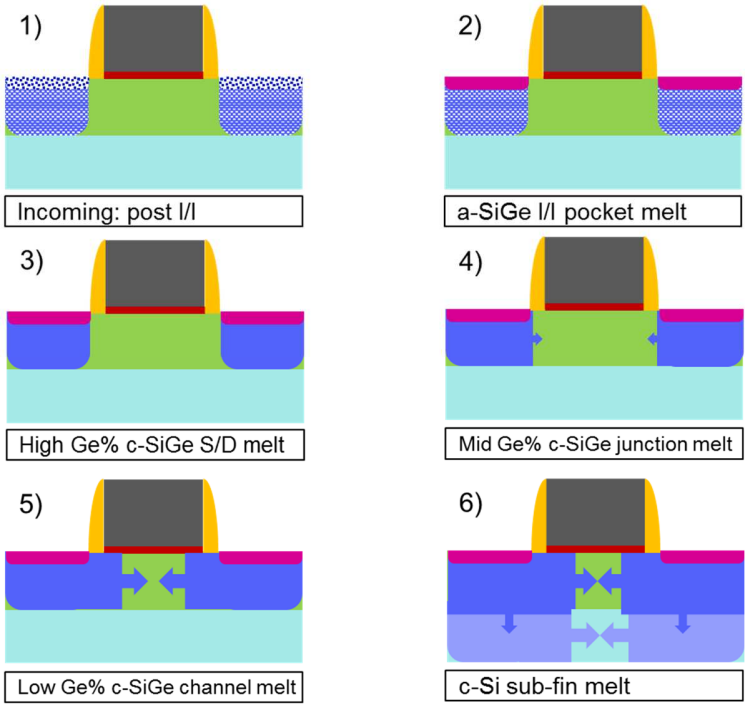

Fig. 16. Schematic illustrating materials melting hierarchy: (1) incoming structure; (2) amorphous SiGe pocket melt; (3) crystalline high-percent-Ge SiGe source/drain melt; (4) crystalline mid-percent-Ge SiGe junction melt; (5) crystalline low-percent-Ge SiGe channel melt; (6) Si subfin melt.

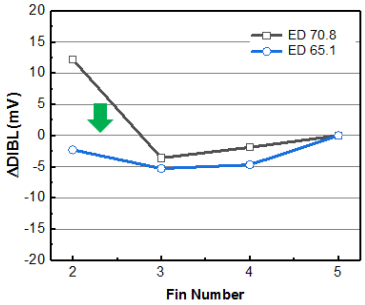

Fig. 17. pFET ΔDIBL dependence on the fin number. pFETs with reduced number of fins annealed at higher temperature. Lowering incident ED by one interval eliminates DIBL degrade.

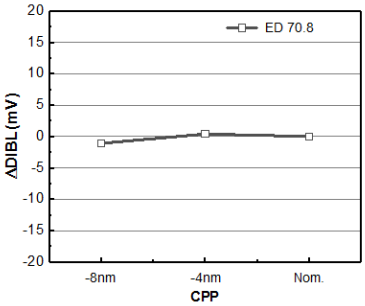

Fig. 18 pFET ΔDIBL dependence on the contacted gate pitch (CPP). No dependence is observed within the studied range suggesting that CPP dependence is weak.