Overlay Performance of Through Si Via Last Lithography for 3D Packaging

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Abstract

Foundry customers and makers of leading-edge devices are evaluating through-silicon via (TSV) for next-generation three-dimensional (3D) packaging. Scaling the diameter of the TSV is a major driver for improving system performance and cost. With smaller TSV diameters, back-to-front overlay becomes a critical parameter because via landing pads on the first metal level must be large enough to include both the TSV critical dimension (CD) and overlay variations.

In this paper we investigate the long term capability of a Dual Side Alignment (DSA) lithography system for printing 5 µm and smaller TSV features. DSA lithography is used to pattern the TSV feature, and Stepper Self Metrology (SSM) is performed to verify the overlay after photoresist development. Multiple stepper lithography fields per wafer and multiple wafers per lot are measured to obtain a statistically significant data set for wafer lot overlay analysis. In addition, multiple wafer lots were processed and measured to establish long term overlay performance and stability. In order to independently verify the SSM overlay data, dedicated electrical structures were designed and placed on a Via Last TSV test chip. These structures allow the TSV diameter and TSV overlay to be measured electrically after lot completion. Vector plots were used to compare the SSM overlay and electrical overlay data.

Introduction

Packaging using TSV is an industry leading process in consumer product related devices such as backside illuminated image sensors (BSI), interposers and 3D memory devices [1]. The various process flows for TSV processing (Via First, Via Middle and Via Last) affect the relative levels of integration required at the foundry and OSAT manufacturing locations. Via Last provides distinct advantages for process integration: it minimizes the impact on Back End of Line (BEOL) processing, and does not require a TSV reveal for the wafer thinning process. Scaling the diameter of the TSV is a major driver for improvement in system performance and cost. Current via last diameters are approximately 30µm with advanced TSV designs at 5 µm [2, 3].

Lithography is one of the critical factors affecting overall device performance and yield for via last TSV fabrication [3]. One of the unique lithography requirements for via last patterning is the need for back-to-front side wafer alignment. With smaller TSV diameters, the back-to-front overlay becomes a critical parameter because via landing pads on the first level metal must be large enough to include both TSV critical dimension (CD) and overlay variations as shown in figure 1. Reducing the size of via landing pads provide significant advantages for device design and final chip size. For this study 5µm TSV's with overlay performance of ≤ 750nm are evaluated.

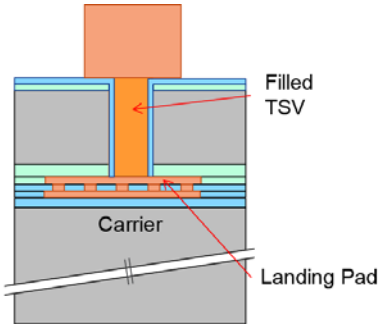

Fig.1: The landing pad on the first level metal must be large enough to include both the TSV critical dimension (CD) and overlay variations.

DSA Alignment and Optical Metrology

Lithography was performed using an advanced packaging 1X stepper with a 0.16 numerical aperture (NA) Wynne Dyson lens. This stepper has a Dual Side Alignment (DSA) system which uses infrared (IR) illumination to view metal targets through a thinned silicon wafer [4]. The naming convention used in this study is that the wafer device side is the front side and the silicon side is the back side. The side facing up on the lithography tool is the back side of the TSV wafer as shown in figure 2.

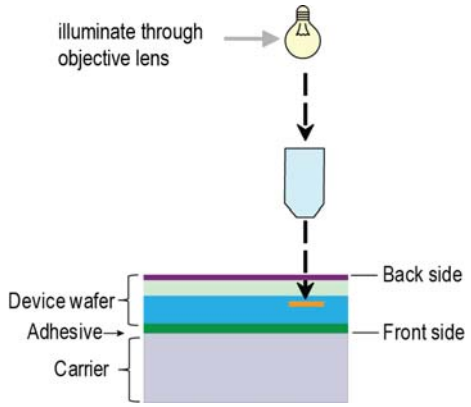

Fig. 2: Off axis alignment configuration with IR illumination and imaging from above the wafer. This configuration is extremely flexible, providing access to the entire wafer for target alignment.

For viewing embedded alignment targets, the method of top IR illumination, shown in figure 2, provides practical advantages for integration with stepper lithography. Since the illumination and imaging are directed from the top, this method does not interfere with the design of the wafer chuck, and does not constrain alignment target positioning on the wafer.

The top IR alignment method illuminates the alignment target from the back side using an IR wavelength that can transmit through silicon (shown as light green in figure 2) and the process films (shown in blue). For this configuration the target (shown in orange) needs to be made from an IR reflective material such as metal for best contrast. The alignment sequence requires that the wafer move in the Z axis in order to shift alignment focus from the wafer surface to the embedded target.

Back-to-front side registration was measured using a metrology package on the lithography tool which uses the DSA alignment system. This stepper self metrology package (DSA-SSM) includes routines to diagnose and compensate for measurement error from having features at different heights. For each measurement site the optical metrology system needs to move the focus in Z between the resist feature and the embedded feature. Therefore angular differences between the Z axis of motion, the optical axis of the alignment camera, and the wafer normal will contribute to measurement error for the tool [4]. The quality of the wafer stage motion is also very important because a significant pitch and roll signature would result in a location dependent error for embedded feature measurement, which would complicate the analysis.

If the measurement operation is repeatable and consistent across the wafer, then a constant error coming from the measurement tool, commonly referred to as tool induced shift (TIS), can be characterized using the method of TIS calibration, which incorporates measurements at 0 and 180 degree orientations. The sum of offsets for the two orientations divided by 2 gives the TIS error [5]. The TIS calibration is effective for many types of measurements for planar metrology. However for embedded feature metrology the quality of measurement and calibration also depend on the quality and repeatability of wafer positioning, including tilt. In previous investigations, the registration data obtained from the current method were self consistent and provided useful feedback for process monitoring [4, 6]. However given the dependencies affecting TIS calibration for embedded feature metrology, it is desirable to confirm the registration result using an alternate metrology method [6]. For in-line metrology it has been difficult to identify an alternate method that rivals the quality of the current method. However later in the wafer process the registration of the completed device can be measured using special electrical test structures as discussed in the next section.

Electrical Detection of TSV Alignment

Electrical verification of TSV alignment is performed after complete processing and relies on the landing position of a TSV on a fork-to-fork test structure in the embedded metal 1. After lithography the TSV, STI (Shallow Trench Isolation) and PMD (pre-metal dielectric) oxides are etched, landing on metal 1. When the TSV processing is complete the Cu filled TSV will make contact with metal 1. In this particular structure the TSV will create a short between two sets of metal forks. Figure 3 shows the schematic layout of this structure for the overlay evaluation in the X direction. A similar structure rotated 90 degrees is used for the Y direction.

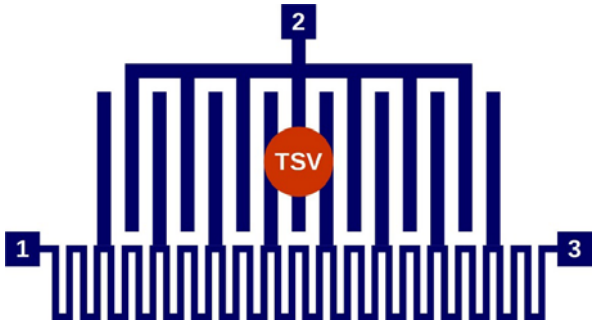

Fig. 3: Schematic layout of the fork structure designed to electrically measure the TSV X direction misalignment with respect to metal 1.

The structure consists of two interlaced metal 1 forks; the top fork has the branches connected to the measurement pad 2; the bottom fork has the branches connected to interior points of a 2-terminal metal 1 meander resistor, $R_{1\text{-}3}$, accessible by pad 1 and pad 3. The bottom fork subdivides this resistor into an integer number of equal resistance units R_u between two neighboring fingers of the fork. R_u can be obtained by dividing the total resistance $R_{1\text{-}3}$, measured on a reference structure without TSV, by N+1, where N is the number of branches of the bottom fork. The pitch of adjacent bottom fork branches defines the distance unit L_u in the X direction as shown in figure 4.

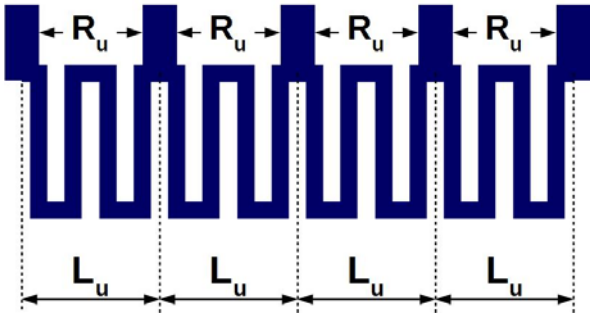

Fig. 4: The resistance of a unit R_u is proportional to the bottom fork pitch L_u.

The manufacturing of the TSV causes the top and bottom metal forks to be shorted together by the TSV. As a consequence, pad 2 is connected through the TSV to points on the meander resistor, thus allowing measurement of two resistances, namely $R_{1\text{-}2}$, between pads 1 and 2, and $R_{2\text{-}3}$, between pads 2 and 3. These resistance measurements are translated to edge locations. For the X-direction, $R_{1\text{-}2}$ is converted to x_{E1}, and $R_{2\text{-}3}$ is converted to x_{E2}. $R_{1\text{-}2}$ and $R_{2\text{-}3}$ have values that are integer multiples of R_u, and the corresponding edge locations have values that are integer multiples of L_u. For the case of ideal TSV alignment, $R_{1\text{-}2} = R_{2\text{-}3}$, which is illustrated in figure 5.

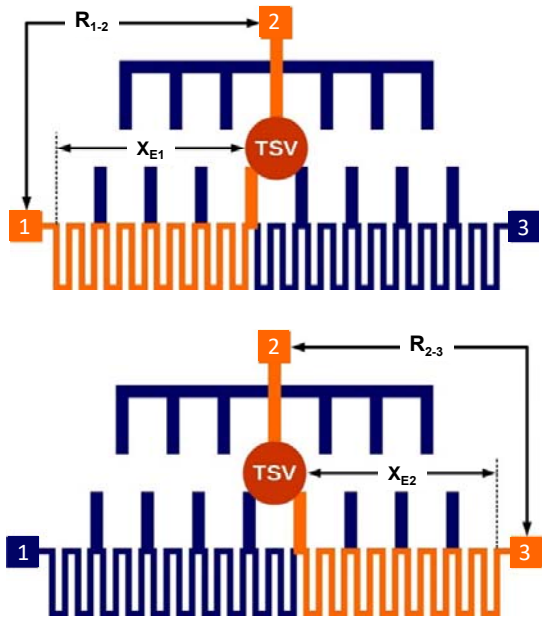

Fig. 5: The TSV connects the two forks which creates two resistances, $R_{1\text{-}2}$ (left) and $R_{2\text{-}3}$ (right) which can be measured separately.

There is an uncertainty in the exact location of the edge of the TSV because it will be anywhere between the shorted fork and the next (open) fork as is indicated by the red arrow in figure 6. The measurement resolution of the structure is limited by L_u, the pitch of the fork branches. In this design, L_u=720nm.

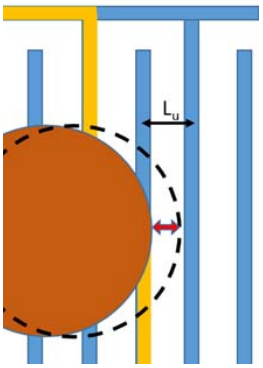

Fig 6: The red arrow indicates the uncertainty of edge location of the fork-to-fork structure.

The measurement resolution can be improved by adding more structures with a pre-defined offset of ¼L_u, ½L_u and ¾L_u to the set. Combining all four sets of resistor data improves the resolution to ¼L_u, which in our case is 180nm (±90nm). The resultant accuracy of this structure depends on the contact resistance between top and bottom forks provided by the TSV; this resistance must be negligible with respect to the unit resistance R_u. Therefore, the fork width is chosen to be reasonably large (180nm) to minimize the contact resistance. To avoid parasitic resistance contributions from the probe-pad contact resistance, pads 1, 2 and 3 are duplicated in the real structure, to allow 4-point resistance measurements of $R_{1\text{-}3}$, $R_{1\text{-}2}$ and $R_{2\text{-}3}$, as shown in figure 7.

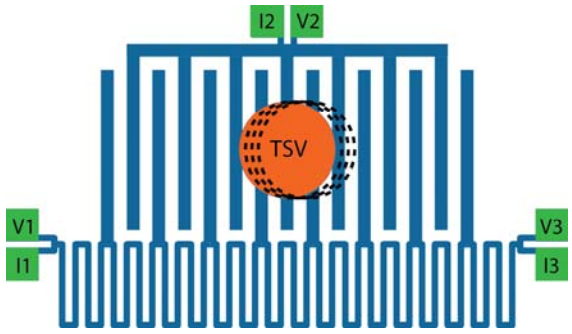

Fig. 7: Graphical representation of shifts in TSV placement. If the TSV edge shifts to contact a new bottom branch then this will be detected as a change in $R_{1\text{-}2}$ or $R_{2\text{-}3}$, with a step pitch of L_u.

An identical structure rotated through 90 degrees is required to gather Y data, y_{E1} and y_{E2}. From all the datasets both overlay error and size of the TSV in both X and Y can be determined.

Experimental Methods

This study investigates image placement performance by examining DSA optical metrology repeatability after TSV lithography, and then comparing this optical registration data with final electrical registration data.

The TSV-last process begins with a 300mm device wafer with damascene metal (metal 1) that is temporarily bonded to a carrier for mechanical support as shown in figure 8. The back side of the silicon device wafer (light green) is thinned by grinding and then polished smooth by CMP. The TSV is imaged in photoresist (red) and is etched through the thinned silicon layer. Figure 8 depicts the complete process flow including the TSV, STI and PMD etch, TSV fill, RDL and de-bonding from carrier. The aligned TSV structure must land completely on the metal 1 pad (dark blue).

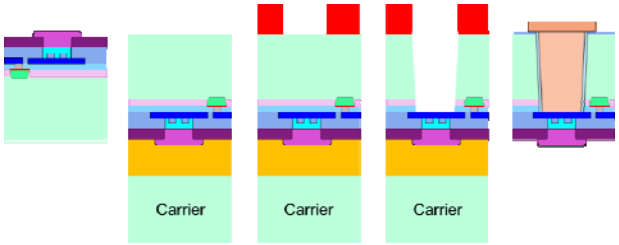

Fig. 8: Representation of complete TSV-last process. From left to right: 1) Completed front-end wafer, 2) Temporary bonding of wafer and backside thinning, 3) TSV-last lithography, 4) TSV etch, 5) TSV filling, RDL and de-bonding from carrier.

TSV lithography is done with a stepper equipped with DSA. The photoresist is a gh-line novolac based positive-tone material requiring 1250mJ/cm^2 exposure dose with a thickness of 7.5µm [6]. The TSV diameter is 5µm, and the silicon thickness is 50µm. TSV etching of the silicon is performed by Bosch etching [7]. Tight control of lithography and TSV etching is required to insure that vias land completely on metal 1 pads as shown in figure 1.

Allowable features for DSA-SSM metrology must conform to the via process requirements for integration. Since

the TSV etch process is very sensitive to pattern size and density, the TSV layer is restricted to one size of via, and the DSA-SSM measurement structure is constructed using this shape. The design of the DSA-SSM measurement structure, shown in figure 9, uses a cluster of 5µm vias with unique grouping and clocked rotation to avoid confusion with adjacent TSV device patterns during alignment.

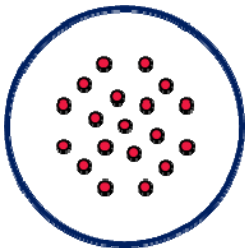

Fig. 9: DSA-SSM overlay structure uses a cluster of 5µm diameter TSV's. The blue ring indicates the landing pad in metal 1 which is the reference layer. The red circles are vias printed in the photo-resist.

DSA camera images of the overlay structure, with two different focus offsets, are shown in figure 10. For this structure the reference metal 1 feature (outlined by the blue ring) and the resist pattern feature (outlined by the red ring) are not in the same focal plane. For a silicon thickness of 50µm, focusing on one feature will render the other feature out of focus. Therefore, each feature must have its own focus offset which is specified in the metrology measurement recipe.

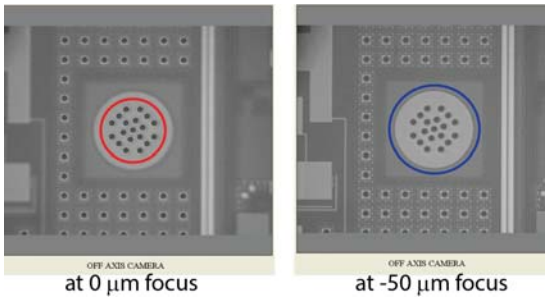

Fig. 10: The left-hand image shows the resist target in focus (outlined in red ring). These are on the top surface (focus at 0 µm). The right-hand image shows the circle of metal 1 in focus at -50 µm (outlined by blue ring). The height difference between the two features is larger than the focal depth of the alignment camera so one of the two is always out of focus.

Optical Registration Process Control

An example vector map for TSV optical overlay measurements is shown in figure 11. The sampling plan of 23 lithography fields with 5 measurements per field gives a total of 115 measurements per wafer, which provides a good statistical sample for monitoring linear grid and intrafield parameters. The full wafer layout contains 262 fields.

In the initial run the overlay settings were optimized using the DSA-SSM metrology feedback and then the parameters were fixed to investigate overlay stability over a nine-week period. Trend charts for mean and 3σ for seven TSV lots are shown in figure 12. Each measurement lot consists of 8 wafers, with 115 measurements per wafer, and all data is corrected for TIS on a per lot basis using measurements of a single wafer at 0 and 180 degree orientations [4]. The lot 3σ is consistently less than 600nm over the nine-week period. There appears to be a consistent small Y mean error (blue diamond) that could be adjusted to improve subsequent overlay results. With a Y mean correction applied the registration data shows mean plus 3σ ≤ 600nm.

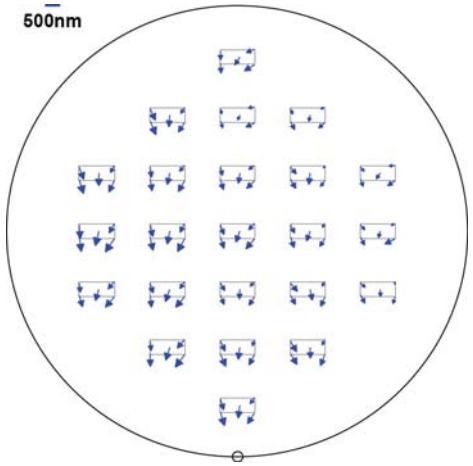

Fig. 11: Example vector plot of TSV overlay measurement on one wafer with sample size of 23 steps and 5 sites per step.

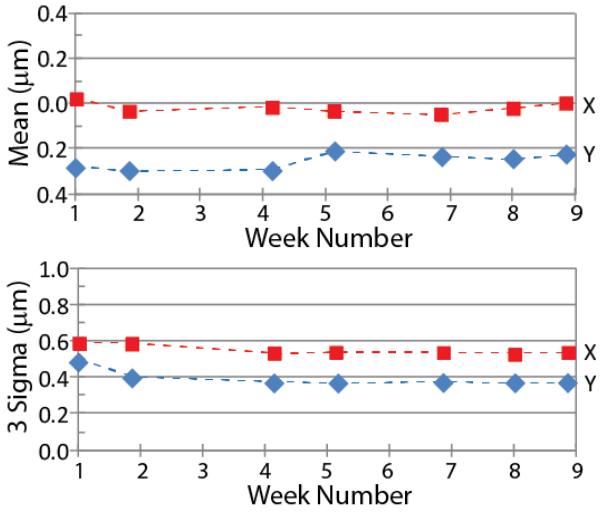

Fig. 12: TSV registration trend charts for lot mean and lot 3σ using in-line optical metrology over nine weeks. The red squares are the X data and the blue diamonds are Y data.

Correlation between Electrical and Optical Registration

Two TSV last test chip wafers were completely processed to the stage that they can be electrically measured. Figure 13 shows vector plots of these wafers with both electrical (black) and optical registration data (blue) for each point. Visually a good match between electrical and optical data can be observed (difference in red). Note that there is only one electrical measurement position per die and that for comparison we have used the optical data obtained from the center of the die, which is closest to the location of the electrical test structures. Table 1 shows the registration numbers that can be extracted from these vector plots confirming a good match between the two metrology methods. It is important to note that an extra translation step is

performed between the optical and the electrical measurement: the TSV etch. In this analysis the TSV etch is assumed to be perfectly vertical. From the data we can conclude that the TSV etch is indeed vertical enough not to interfere with the overlay data. Otherwise this would show as translation or scaling effects between the two metrology methods.

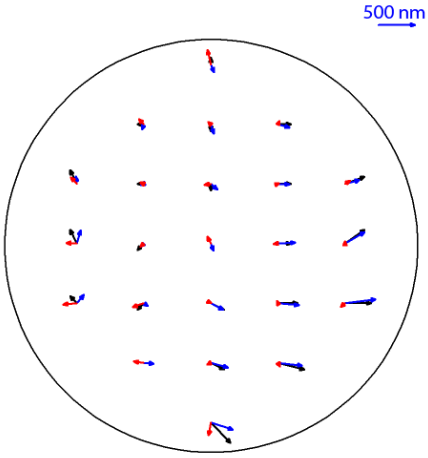

Fig 13(a): Vector plot of 23 measurements across wafer D10. Blue is optical registration data, black is electrical registration data, and the red indicating the difference between the two.

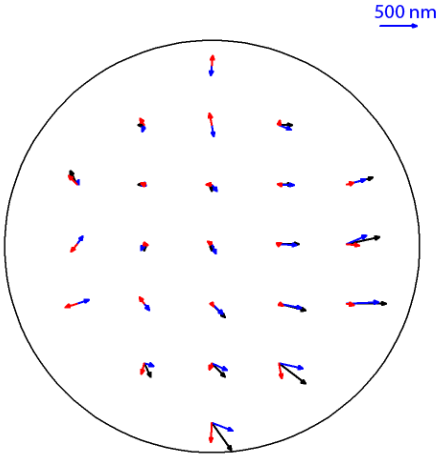

Fig 13(b): Vector plot of 23 measurements across wafer D17. Blue is optical registration data, black is electrical registration data, and the red indicating the difference between the two.

Table1: Statistical summary of electrical and optical registration data for wafer D17 and wafer D10, confirming a close match. All numbers are in units of nm.

Metrology Type	Wafer D17				Wafer D10			
	Mean		1σ		Mean		1σ	
	X	Y	X	Y	X	Y	X	Y
Electrical	137	-51	186	121	90	-4	163	107
Optical	146	-41	132	78	140	-14	129	82
Difference	9	10	76	100	50	-10	63	68

Conclusions

The lithographic method for TSV alignment to embedded targets was evaluated using in-line stepper self metrology, with TIS correction. Registration data was collected over a nine-week period to characterize the stability of TSV alignment. With corrections applied, the registration data demonstrates mean plus $3\sigma \leq 600$nm. The in-line optical registration data was then correlated to detailed electrical measurements performed on the same wafers at the end of the process to provide independent assessment of the accuracy of the optical data. Good correlation between optical and electrical data confirms the accuracy of the in-line optical metrology method, and also confirms that the TSV etch through 50µm thick silicon is vertical.

Acknowledgments

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